

3-Bit SAR ADC

Design a 3-bit successive approximation ADC. Meet the following specifications:

- Operation up to 1 MSPS (mega-sample-per-second)
- I/O:
 - Dout: 3-bit parallel latched digital output
 - Vin: input voltage, 1V peak-to-peak amplitude. Ideally 0V to 1V, but you are allowed up to 500mV offset if required due to your comparator ICMR
 - clk: one input clock, at a frequency of your choice
 - Vref: optional 1V reference input voltage, does not need to be buffered (not required if you use the current-scaling DAC)
 - Vdd & GND (either explicit I/O or implied with global nodes)
- Sample & hold: a S/H of the input voltage is NOT required for this assignment. Note that you will likely have to add a S/H when using this block in your final project.

With the following design constraints:

- Power supplies: $V_{dd} = 3.3V$, $V_{ss} = 0V$
- Re-use any comparator and DAC that YOU designed in previous assignments
- Sample (4-bit) Verilog code and a symbol for the SAR are available on the course library (ams_5007_ref HW8_SAR_ADC H2_SAR). You are welcome to edit this code or create your own.
- Use as many additional nmos and pmos devices as desired (but should be doable with only existing blocks, possibly with modification, and the SAR).

Turn in

- Top level ADC schematic as well as top schematic of internal DAC and comparator
- Final code for SAR and synthesized schematic & layout
- Final top level layout with results showing LVS clean
- Mixed-signal (ideal Verilog blocks) simulation with a ramp input voltage, 1V amplitude, rise time of 50us, sampled at 1 MSPS (showing digital output and ramp input)
- Final extracted analog simulation with one input voltage step to show correct outputs at two input levels, $\frac{1}{4}$ and $\frac{3}{4}$ full scale input