LECTURE 11 – HARMONIC BALANCE ANALYSIS FOR NONLINEAR SIMULATIONS

L11.1. HARMONIC BALANCE FUNDAMENTALS

The s-parameter analysis we have done so far is based on linear parameters: for a single sinusoidal excitation, the output will contain only the same sinusoidal frequency. Soon we will analyze oscillators, in which the input is a DC voltage, while the desired output is an RF sinusoidal voltage, with a number of harmonic frequency components present. The many frequencies present in the output voltage with a DC input were a result of the nonlinear characteristics of the transistor.

There are two ways to analyze nonlinear circuits: in time domain (such as in Spice) or in frequency domain by separately considering the response of the circuit to a number of harmonics of the fundamental input frequency. Time-domain techniques have the following problems at microwave frequencies:

1. It is difficult to include linear matching and other networks that are dispersive (frequency-dependent);
2. Long integrations accompanied by intensive computations and large truncation errors are necessary when the time-constant of circuit is large compared to the period of the excitation frequency; and
3. Each linear or nonlinear reactive element in the circuit adds a differential equation to the set of equations that describe the circuit.

Instead, in microwave circuit simulators, multiport theory combined with frequency-domain simulations is used. Consider the circuit in Figure L11.1a, which contains some nonlinear active device that requires biasing (a diode or transistor) and linear matching and filtering networks. The circuit elements can be regrouped in such a way that all linear components (including linear parts of the active device) are contained in one multiport network with N+2 ports, while the nonlinear components are grouped on a non-linear multiport network with N ports, Figure L11.1b. Each of the N ports contains all frequency components of interest, and the current continuity can be expressed as

\[
\begin{bmatrix}
I_{1,0} \\
I_{1,1} \\
I_{1,2} \\
\vdots \\
I_{N,K}
\end{bmatrix} + \begin{bmatrix}
\tilde{I}_{1,0} \\
\tilde{I}_{1,1} \\
\tilde{I}_{1,2} \\
\vdots \\
\tilde{I}_{N,K}
\end{bmatrix} = \begin{bmatrix}
0 \\
0 \\
0 \\
\vdots \\
0
\end{bmatrix},
\]

(11.1)

where the index 1..K represents the harmonic of the 1\textsuperscript{st} through N-th port node. The basic principle of harmonic balance is to solve the circuit to find port voltages such that Eq.(11.1) is satisfied, i.e. such that the currents in the nonlinear and linear sub-network connecting ports are identical.
Figure L11.1. A nonlinear microwave circuit block diagram (a) and re-grouped elements of the circuit for harmonic balance analysis (b).

The sources at the input and output ports are given for generality, and their impedances are included in the linear sub-circuit. Usually, a sinusoidal source is present only at the input, while the output port contains only DC bias (such as in a FET amplifier). The voltages and currents at the \( N \) ports contain the DC component, as well as \( K \) harmonics of the fundamental excitation frequency, and it is assumed that these \( K \) harmonics adequately describe the nonlinear circuit. In many cases, the choice of \( K \) is critical to accurate modeling.

The linear sub-circuit admittance \((Y)\) matrix is a \((N+2)\) times \((N+2)\) matrix relating the \((N+2)\) currents at the \( K \) harmonics to the \((N+2)\) port voltages at the \( K \) harmonics:

\[
\begin{bmatrix}
I_{N+1} \\
\vdots \\
I_{N+2}
\end{bmatrix} =
\begin{bmatrix}
Y_{1,1} & \cdots & Y_{1,N+2} \\
\vdots & \ddots & \vdots \\
Y_{N+2,1} & \cdots & Y_{N+2,N+2}
\end{bmatrix}
\begin{bmatrix}
V_1 \\
\vdots \\
V_{N+2}
\end{bmatrix},
\tag{11.2}
\]

where each of the bold-faced current and voltage sub-matrices contain the \( K \) harmonics and are given by
The Y submatrices are diagonal matrices with elements given by

\[
Y_{m,n} = \begin{bmatrix}
Y_{m,n}(0) & 0 & \cdots & 0 \\
0 & Y_{m,n}(\omega) & \cdots & 0 \\
\vdots & \vdots & \ddots & \vdots \\
0 & 0 & \cdots & Y_{m,n}(K\omega)
\end{bmatrix}
\]

The two voltage harmonic vectors corresponding to the input and output ports can be written as an “excitation vector”:

\[
\begin{bmatrix}
V_{b_1} \\
V_s \\
V_{N+1} \\
V_{N+2}
\end{bmatrix} = \begin{bmatrix}
Y_{1,1} & Y_{1,N+1} & \cdots & Y_{1,N} \\
\vdots & \vdots & \ddots & \vdots \\
Y_{N,1} & Y_{N,N+1} & \cdots & Y_{N,N}
\end{bmatrix} \begin{bmatrix}
V_1 \\
\vdots \\
V_N
\end{bmatrix},
\]

where \(V_{b_1}\) and \(V_{b_2}\) are bias voltages at the input and output ports (N+1) and (N+2), and \(V_s\) is the input excitation voltage at port (N+1). Port (N+1) has both an AC and DC input, while port (N+2) has only a DC bias, such as in the case of a FET amplifier. If the input is not sinusoidal, the vector on the right would include harmonic voltages instead of 0s. Now the Y matrix in Eq.(11.2) can be partitioned and expressed in terms of a 2x2 excitation matrix and a NxN circuit matrix:

\[
\begin{bmatrix}
I_1 \\
\vdots \\
I_N
\end{bmatrix} = \begin{bmatrix}
Y_{1,N+1} & Y_{1,N+2} \\
\vdots & \vdots \\
Y_{N,N+1} & Y_{N,N+2}
\end{bmatrix} \begin{bmatrix}
V_{N+1} \\
V_{N+2}
\end{bmatrix} + \begin{bmatrix}
Y_{1,1} & \cdots & Y_{1,N} \\
\vdots & \vdots & \vdots \\
Y_{N,1} & \cdots & Y_{N,N}
\end{bmatrix} \begin{bmatrix}
V_1 \\
\vdots \\
V_N
\end{bmatrix}.
\]

The above matrix equation can be re-written as \(I = I_s + Y_{N\times N}V\). The circuit-theory meaning of this equation is as follows. \(I_s\) represents N current sources in parallel with the N ports. The first term in the matrix equation transforms the excitations at the input and output ports into these
parallel current sources, as shown in Figure L11.3. This eliminates the need to keep track of the (N+1)st and (N+2)nd ports. Therefore, the harmonic-balance equations are expressed in terms of only the currents in the N ports connected to the nonlinear elements. The currents in the nonlinear elements, \( \tilde{I} \) can be a result of non-linear capacitors or non-linear resistors.

**Figure L11.3.** Re-grouped equivalent circuit, with the excitation (AC and DC) signals represented as equivalent current sources distributed in the N ports.

Now what remains to be answered is how the different nonlinear elements are included in the analysis. In a microwave diode, there are two nonlinearities: the resistance (slope of the IV curve) and the junction capacitance. In a transistor, there are a number of nonlinear elements, for example the voltage-dependent current source and the output capacitance are nonlinear elements. A voltage-controlled current source can be described by the very general time-domain equation

\[
i_{g,n}(t) = f_n(v_1(t), v_2(t), ..., v_n(t))
\]

which can be Fourier-transformed to obtain an expression in frequency domain:

\[
\mathcal{F}\{i_{g,n}(t)\} \rightarrow I_{G,n}.
\]

A vector of all \( n=N \) currents is the input \( I_G \) to our harmonic balance equation.

In a nonlinear capacitor, the charge can be expressed in terms of voltages in time domain, and then a Fourier transform performed:

\[
q_n(t) = f_{qn}(v_1(t), v_2(t), ..., v_n(t)) \quad \text{and} \quad \mathcal{F}\{q_n(t)\} \rightarrow Q_n,
\]

where the charge vector input to the harmonic balance matrix equation is
where $N$ is the number of nonlinear capacitors and $K$ is the number of harmonic frequencies. The current in the nonlinear capacitor is the time derivative of the charge waveform, which corresponds to a multiplication with $j\omega$ in the time-harmonic domain:

$$i_{c,n}(t) = \frac{dq_{nn}(t)}{dt} \leftrightarrow j\omega Q_{n,k},$$

which can be expressed in matrix form by introducing a “harmonic frequency” matrix which is diagonal and has $N$ cycles of $[0, \omega, 2\omega, \ldots, K\omega]$ along the diagonal, and is a large $(K+1)N \times (K+1)N$ matrix. The capacitor current vector input to the harmonic balance matrix equation can now be written as

$$I_C = j\Omega Q.$$

where $\Omega$ is a diagonal matrix of frequencies $\omega, 2\omega, \ldots, K\omega$. The nonlinear capacitor and nonlinear resistor/conductor currents are now included in Eq.(11.1) as follows:

$$\mathbf{F}(\mathbf{V}) = I_s + Y_{N\times N} \mathbf{V} + j\Omega Q + I_0 = 0. \quad (11.3)$$

This equation is a test to determine the accuracy of the current continuity at the nodes of the circuit separated into a linear and nonlinear subcircuit, and assuming a trial set of voltages at the ports. If Eq.(11.3) holds, the voltages of vector $\mathbf{V}$ are the solutions. $\mathbf{F}(\mathbf{V})$ is the current error vector of the harmonic balance equation (11.3).

Each of the $(K+1)$ frequency components of $\mathbf{V}$ at each port is a variable, with a real and imaginary (or phase and amplitude) part, resulting in $2N(K+1)$ unknowns to solve for. As an example, in a FET multiplier, there are 3 nonlinear ports, and usually no less than 8 frequencies are needed for a reasonably accurate solution (assuming a good transistor model). Therefore, in the multiplier harmonic balance solution, there are 54 unknown voltages to solve for. What numerical methods are used to obtain these solutions?

A number of numerical methods seem like a reasonable approach, for example, optimization, Newton’s method (using the Jacobian of $\mathbf{F}(\mathbf{V})$), and the more physically intuitive splitting and reflection methods. The reflection method was introduced by Kerr to study harmonically-pumped mixers, and this will be a topic of discussion in one of the next lectures.
The splitting method starts with an estimate $V^0$ of the solution. Then $V^0$ is Fourier-transformed to obtain $v^0_x(t)$, and $v^0_x(t)$ is substituted into the nonlinear element equations to obtain current and charge waveforms. These are then Fourier transformed. $I^0$ is then estimated as $-\tilde{I}^0$ and a new voltage vector is found form the linear subcircuit:

$$V^* = Y^{-1}_{N×N}(I^0 - I_S)$$

The new estimate of $V$ is then found: $V^1 = sV^* + (1-s)V^0$. Here, $s$ is a real number referred to as the splitting coefficient and is a constant that is determined empirically, but is usually 0.2 and never bigger than 1 (small values yield slow convergence, while larger ones can give unstable solutions). Next, the process is repeated with $V^0$ replaced by $V^1$ and so on until a pre-specified satisfactory value of the error.

L11.2. HARMONIC BALANCE EXAMPLE

As a simple illustration of the harmonic balance method, consider a detector circuit (we will study detectors shortly), as shown in Figure L11.4a. The circuit is rearranged into linear and nonlinear subnetworks and the excitation, Figure L11.4b. Subsequently, following the discussion above, the excitation is represented as a current source effectively transforming the circuit to an equivalent one-port. We will assume that the diode is ideal and has no series resistance or junction capacitance. Therefore, only one nonlinear element exists, so $N=1$, and the vector $V = V_1$. The admittance matrix of the linear embedding network, $Y_m$, can be written as

$$Y_m = \begin{bmatrix} Y_{1,1} & Y_{1,2} \\ Y_{2,1} & Y_{2,2} \end{bmatrix}, \text{ and } I_S = I_{S,1} = Y_{1,2}V_2.$$  

When $V_2$ is transformed through the $Y$ network, the equivalent circuit from Figure L11.4c results. The vector $V_2$ consists only of the fundamental frequency source $V\cos \omega t$ and the DC bias source:

$$V_2 = \begin{bmatrix} V_b \\ V \\ 0 \\ \vdots \end{bmatrix}.$$  

Now an initial estimate of either $V(t)$ or $V_1$ is needed, and usually for a diode it is taken as a clipped sinusoid (clipped at about 0.6V). The Fourier transform of $V(t)$ gives the components of $V_1$. The diode current is given by the ideal diode equation

$$i_{g,1}(t) = I_S (\exp(v_1(t)/V_T) - 1)$$  

and since there is no capacitance, $q(t)=0$.

The current error vector is now

$$F(V) = Y_{1,2}V_2 + Y_{1,3}V_1 + I_{G,1}.$$  


In order to solve Eq.(11.4) the splitting algorithm can be used as follows:

- Invert \( Y_{1,1} \) matrix (diagonal) to generate embedding impedance matrix
- form an initial estimate of \( v_1(t) \) as a sinusoid at the fundamental frequency clipped by 0.6V with a DC offset of the bias voltage
- calculate \( i_{g,1}(t) = I_s \left( \exp(v_1(t)/V_T) - 1 \right) \)
- Perform Fourier transforms of \( i_{g,1}(t) \) and \( v_1(t) \), which gives \( I_G^0 \) and \( V_1^0 \)
- Assume \( I = -I_G^0 \) and form \( V'' = \mathbf{Z}_{1,1}(1 - I_s) \)
- Form the new estimate of \( V_1 \) as \( V_1^i = sV'' + (1 - s)V_1^0 \)
- Perform inverse Fourier transform of \( V_1^i \) to obtain a new estimate of \( v_1(t) \), repeat step 3 until convergence is achieved.
- If there is an instability, reduce \( s \).

The two other Y parameters of the admittance matrix that were not mentioned above can be used to find the input current from the source \( (I_2) \) once \( V_1 \) is known. \( I_2 \) is then used to find the input power, the power dissipated in the source and the source impedance that was previously included in the linear network.

\[
\begin{align*}
I(V) & \quad \text{Input voltage} \\
I & \quad \text{Current} \\
V_1 & \quad \text{Input voltage} \\
V_2 & \quad \text{Output voltage}
\end{align*}
\]

**Figure L11.4.** (a) Video detector circuit. (b) Rearranged circuit with linear and nonlinear subnetworks, and (c) with two-port equivalent circuit reduced to one-port.