The goal of this project is to (1) go through the process of implementing a nonlinear transistor model in ADS/AWR with and without package parasitics; (2) Design a power amplifier and (3) learn how to do nonlinear harmonic balance simulations and understand the limitations of the models.

Part 1. Implementing the TOM3 Model and Verifying DC IV Curves

In the first part of this project you will implement the TOM3 device model for the Filtronic FPD3000 in ADS/MWO. In addition to the TOM3 die model an RLC circuit must also be constructed to represent the SOT89 package. Model performance will be verified by simulating IV curves and S-parameters and comparing results to published IV curves and S-parameters. This takes a bit of time, count on about 1 hour to set up the model.

Note that the following files will be referenced:

<table>
<thead>
<tr>
<th>Title</th>
<th>Filename</th>
</tr>
</thead>
<tbody>
<tr>
<td>[3] FPD3000 S-parameters at 5V, 300mA</td>
<td>FPD_5V_300mA.s2p</td>
</tr>
</tbody>
</table>

John Hoversten, a former graduate student in my group, has made an additional set of hints for a systematic approach to model building in MWO. You can consider using hierarchical schematics for this project and follow John’s approach (posted in a separate file). This means that, for example, you can make the TOM3 model one sub-circuit and place it inside the SOT89 package sub-circuit. Then you can use the combined TOM3+SOT89 sub-circuit in simulation circuits. This approach is illustrated in [4]. Also included in [4] are steps and sample results obtained for this project in MWO. Read the device datasheet [5] for notes on device operation, bias, and performance.

The parameters for the TOM3 model are given in [1]. However, this model has been extracted to represent only the device behavior, and does not include the effects of bond wires and other external package parasitics. The published IV curves on page 8 include the effect of the fixture in which the device was characterized. This test fixture can be constructed as shown on page 3. The IV curves simulated for this model will exactly match those published on page 8 when the model is correctly implemented.

Procedure for implementing the model for this particular device:
Find the TOM3 element in ADS/MWO and place it in a schematic. In ADS, you need the model and the device. Most of the parameters go into the model, but some go into the device (scaling parameters, e.g.)

Enter in the parameters on page 5 into the properties of the TOM3 element.

Notes:
- In MWO click the "Show Secondary" button to view all model parameters.
- Be careful about the units on parameters (e.g. uF vs. nF).
- Leave unspecified parameters at their default value.
- The units of the IS parameter are not defined, but make no practical difference.

Draw the measurement fixture circuit of page 3 and add the TOM3 model.

Simulate the IV curves of the device with the fixture and verify against those on page 8.

Notes:
- In MWO use the "IVCURVE" element found in "MeasDevice" and connect the "Step" and "Sweep" ports to the gate and drain, respectively. Create a new graph and add the "IVCurve" measurement found in "Nonlinear"->"Current"->"IVCurve".
- Do not continue until the curve matches those on page 8. Agreement should be excellent.

Part 2. Implementing the SOT89 Package and Verifying S-Parameters

The device is not sold in the measurement fixture from part 1, but instead a standard SOT89 package is used. A schematic representation of this packaged can be found in [2].

Simulation to find S-parameters of the nonlinear model will require use of harmonic balance. The transistor model must be DC-biased at gate and drain the desired bias point. Use an idealized bias tee (1H ideal inductor and 1F ideal capacitor) to avoid the complexity of bias tee design. The measured and simulated S-parameters will not agree very well, but should show similar trends over frequency and bias point.

Procedure:
(1) Draw the SOT89 fixture circuit and add the TOM3 model.
(2) Add an ideal bias tee and voltage sources at the gate and drain.
(3) Select an S-parameter data file (e.g. [3]) for comparison and then bias the model with similar drain voltage and quiescent current.

Notes:
- Vgg used in the measured S-parameter file will likely not produce the exact drain current in the model. Adjust Vgg to achieve the correct current.
- In MWO right click on the schematic name and select "Add Annotations", then choose "DCIA" to show DC currents into each node on the schematic (useful for verifying quiescent bias point).
- This TOM3 model indicates excessive gate current (>200uA) that is not physical and does not match the measured data in the S-parameter files. There is nothing we can do about this error.
(4) Plot measured and simulated S-parameters on the same plot.
Part 3- Class-A Power Amplifier

(1) Use the device specs at the higher bias point. Use procedure from notes (class) to find $R_{opt}$, choosing 5V and 300mA between 1 and 4GHz.

(2) Import the device component TOM3 model

(3) Run a harmonic balance simulation. You can start by choosing 10 harmonics and then later test convergence with fewer. You will need to add bias (chokes and supplies, note direction of supplies) and a sinusoidal drive. You will also have to insert a current probe. This is under the probe component, note that it has a direction. In MWO, you can start by importing the High-Power BJT amplifier example.

(4) Plot the load line as $\text{vs}(t_\text{s}(I_{ds,i}), t_\text{s}(V_d))$ – it looks interesting

(5) Plot the harmonic content at the output. You may need to use the help for harmonic balance. You will need to define an equation for the output power. Because now there are more than one frequency, the variables will be arrays, so for example, to specify the 3rd harmonic of the voltage, you would call it $V[3]$. The output power spectral plot is a function, e.g. $P_{\text{out}}=10*\log_{10}(\text{pspec}(V_{\text{out}},0,I_{\text{out},i}))$

(6) Plot $P_{\text{out}}$ vs. $P_{\text{in}}$. At what level does the device reach 1-dB compression?

(7) Plot the drain efficiency as a function of input power. You have to define a few equations to do this.

(8) Examine what happens to the time-domain waveforms as you drive the amp harder.

Part 4- Ideal Switch Class-E PA

(1) The output capacitance is found from $C_{ds}$ in parallel with $C_{gd}$ (from device model). Use an ideal switch in parallel with the output capacitance (as in the lecture) to model an ideal class-E amplifier at 1GHz. What is the class-E max frequency of operation for this device? Use the currents and voltages from the DC simulation in Part 3. Your circuit should look like the one below, approximately.

(2) In ADS, the switch can be found in the parts under System Switch and Algorithmic component. It specifies the on and off resistance and a finite slope during turn-on. To get close to an ideal switch, you need to set the voltages $V1$ and $V2$ close to each other – this means that the voltage waveform is changing only between these values and is closer to an ideal step.

(3) In Microwave Office, there is no ideal switch element, but you can implement one as described at the end of this part. Thanks to my graduate student Asmita Dani who validated this approach and wrote up step-by-step instructions.

(4) Calculate the elements of the output class-E network (lumped is ok, even if it is not realistic – in a real design we would convert to transmission lines). Use a series resonant circuit at 10GHz as the open for all higher harmonics.

(5) Perform a harmonic-balance simulation (HB) with 10 harmonics. Use a sinusoidal voltage drive for the switch ($V_{-1\text{tone}}$ under the frequency domain source component in ADS)

(6) Plot the current and voltage of the switch in time domain. To do that, you have to add a current probe. This is under the probe component, note that it has a direction.

(7) Plot the harmonics of the output power. What is the ratio of the drain bias to the output voltage across the real part of the class-E load?
(8) Find out how the number of harmonics in HB affects your results. How many harmonics are sufficient to simulate this circuit?

(9) Calculate the output efficiency and simulate it to see that it is what you expect.

A few other things you can do are:
- Compare with a nonlinear model simulations where you bias the device in class B and drive it hard.
- It is to change the load by 5% for both real and imaginary parts and examine the effect on the efficiency and time-domain waveforms.

**Implementing an ideal switch in Microwave Office:**

1. The first step to design an ideal switch is to know the on-state resistance of the device you will be using. Define this on-state resistance as an equation in “global definitions” in AWR environment (Ron = the value). “Global definitions” allows you to use this variable in all the schematics without making you define it in every single schematic.

2. Once the Ron is defined, open a circuit schematic and name it e.g. “Switch”. Click on the elements icon on top and type DYN_VCCS and place it on the schematic. For a switch design, you will want a voltage controlled current source. For this element, specify the Type as "Current Source". As the switch will represent a three-terminal transistor device, we need 3 nodes.

3. In the equation part of the DYN_VCCS, specify the following equation: "A1*V0*V1". This equation says that there is a variable A1 on which the voltages depend. Specify A1 = 1/Ron for this element. Now, flip the element so that the current source is on the right side like a transistor model. Voltage V1 is between nodes 3 and 4 resembling the gate of the device and V0 is the current source between nodes 1 and 2 resembling the drain of the device. Connect 50 ohm terminations with port 1 on node 3, port 2 on node 1 and port 3 for nodes 4 and 2.

4. This is the ideal switch element which corresponds to the intrinsic transistor without any output capacitance. Now open a new schematic and name is switch_implement. Place the 3 port subcircuit “Switch” in this schematic. Connect V_METER element in parallel on ports 1 and 2 to monitor the voltage. Place I_METER at port 2 in series. Connect a DC voltage source to the other end of this I_METER with some voltage on it, eg. 28 V. At port 1, place a V_PLS element for controlling the current source in terms of duty cycle with Off State voltage (0V) and on state voltage (1V). You can change the duty cycle by making a swept variable D to vary from 0.05 to 0.95 (use the SWPVAR element).

5. As DT should be in nS, the duty cycle, D is divided by the switching frequency in GHz. The frequency is 1GHz, and DT = D/1. For the V_PLS element, type TW = DT for the element. Also, type the Amplitude to be 1V which will be the On state of the switch.

6. Next, open a graph and put the measurement I_time found in nonlinear<current section. You can also add V_time measurement found in nonlinear<voltage section. In order to get an ideal switching characteristic, go to default circuit option<harmonic balance under project bar and make the number of harmonics for tone 1 large. Simulate the project and open the variable tuner. By changing the duty cycle, you should see the switching window increase and decrease.