Introduction to Power Electronics
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Lecture 15
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6.1. Circuit Manipulations

Begin with buck converter: derived in Chapter 1 from first principles

• Switch changes dc component, low-pass filter removes switching harmonics
• Conversion ratio is $M = D$
6.1.1. Inversion of source and load

Interchange power input and output ports of a converter

Buck converter example

\[ V_2 = D V_1 \]
Inversion of source and load

Interchange power source and load:

\[ V_2 = DV_1 \quad \quad V_1 = \frac{1}{D} V_2 \]
Realization of switches as in Chapter 4

- Reversal of power flow requires new realization of switches
- Transistor conducts when switch is in position 2
- Interchange of $D$ and $D'$

$$V_1 = \frac{1}{D} V_2$$

Inversion of buck converter yields boost converter
6.1.2. Cascade connection of converters

\[ V_1 = M_1(D) V_g \]

\[ V = M_2(D) V_1 \]

\[ \frac{V}{V_g} = M(D) = M_1(D) M_2(D) \]
Example: buck cascaded by boost

\[
\frac{V_1}{V_g} = D
\]

\[
\frac{V}{V_1} = \frac{1}{1 - D}
\]

\[
\frac{V}{V_g} = \frac{D}{1 - D}
\]
Buck cascaded by boost: simplification of internal filter

Remove capacitor $C_1$

Combine inductors $L_1$ and $L_2$

Noninverting buck-boost converter
Noninverting buck-boost converter

![Diagram of the Noninverting buck-boost converter with subintervals 1 and 2.]
Reversal of output voltage polarity

**noninverting buck-boost**

**inverting buck-boost**
Reduction of number of switches: inverting buck-boost

Subinterval 1

\[ V_g \]

\[ i_L \]

\[ V \]

\[ V \]

Subinterval 2

\[ V_g \]

\[ i_L \]

\[ V \]

\[ V \]

One side of inductor always connected to ground — hence, only one SPDT switch needed:

\[ \frac{V}{V_g} = -\frac{D}{1-D} \]
Discussion: cascade connections

- Properties of buck-boost converter follow from its derivation as buck cascaded by boost
  
  Equivalent circuit model: buck $1:D$ transformer cascaded by boost $D':1$ transformer
  
  Pulsating input current of buck converter
  
  Pulsating output current of boost converter

- Other cascade connections are possible
  
  Cuk converter: boost cascaded by buck
6.1.4. Differential connection of load to obtain bipolar output voltage

Differential load voltage is

\[ V = V_1 - V_2 \]

The outputs \( V_1 \) and \( V_2 \) may both be positive, but the differential output voltage \( V \) can be positive or negative.
Differential connection using two buck converters

Converter #1 transistor driven with duty cycle $D$

Converter #2 transistor driven with duty cycle complement $D'$

Differential load voltage is

$$V = DV_g - D'V_g$$

Simplify:

$$V = (2D - 1)V_g$$
Conversion ratio $M(D)$, differentially-connected buck converters

$$V = (2D - 1)V_g$$
Simplification of filter circuit, differentially-connected buck converters

Original circuit

Bypass load directly with capacitor

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Chapter 6: Converter circuits
Simplification of filter circuit, differentially-connected buck converters

Combine series-connected inductors

Re-draw for clarity

H-bridge, or bridge inverter

Commonly used in single-phase inverter applications and in servo amplifier applications
Differential connection to obtain 3Ø inverter

With balanced 3Ø load, neutral voltage is

\[ V_n = \frac{1}{3} (V_1 + V_2 + V_3) \]

Phase voltages are

\[ V_{an} = V_1 - V_n \]
\[ V_{bn} = V_2 - V_n \]
\[ V_{cn} = V_3 - V_n \]

Control converters such that their output voltages contain the same dc biases. This dc bias will appear at the neutral point \( V_n \). It then cancels out, so phase voltages contain no dc bias.
3Ø differential connection of three buck converters

\[ V_g \]

\[ + \]

\[ - \]

\[ V_1 \]

\[ + \]

\[ - \]

\[ V_2 \]

\[ + \]

\[ - \]

\[ V_3 \]

\[ + \]

\[ - \]

\[ V_n \]

\[ + v_{bn} \]

\[ - \]
3Ø differential connection of three buck converters

Re-draw for clarity:

“Voltage-source inverter” or buck-derived three-phase inverter
The 3Ø current-source inverter

- Exhibits a boost-type conversion characteristic
Single-input single-output converters containing one inductor

- Use switches to connect inductor between source and load, in one manner during first subinterval and in another during second subinterval.
- There are a limited number of ways to do this, so all possible combinations can be found.
- After elimination of degenerate and redundant cases, eight converters are found:
  - dc-dc converters
    - buck, boost, buck-boost, noninverting buck-boost
  - dc-ac converters
    - bridge, Watkins-Johnson
  - ac-dc converters
    - current-fed bridge, inverse of Watkins-Johnson
Converters producing a unipolar output voltage

1. **Buck**
   \[ M(D) = D \]

\[ M(D) = \frac{1}{1 - D} \]

2. **Boost**

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Chapter 6: Converter circuits
Converters producing a unipolar output voltage

3. **Buck-boost**
   
   \[ M(D) = -\frac{D}{1-D} \]

4. **Noninverting buck-boost**
   
   \[ M(D) = \frac{D}{1-D} \]
Converters producing a bipolar output voltage suitable as dc-ac inverters

5. Bridge

\[ M(D) = 2D - 1 \]

\[ M(D) = 2D - 1 \]

6. Watkins-Johnson

\[ M(D) = \frac{2D - 1}{D} \]

\[ M(D) = \frac{2D - 1}{D} \]
Converters producing a bipolar output voltage suitable as ac-dc rectifiers

7. Current-fed bridge
   \[ M(D) = \frac{1}{2D - 1} \]

8. Inverse of Watkins-Johnson
   \[ M(D) = \frac{D}{2D - 1} \]
Several members of the class of two-inductor converters

1. Ćuk
   \[ M(D) = -\frac{D}{1 - D} \]

2. SEPIC
   \[ M(D) = \frac{D}{1 - D} \]
Several members of the class of two-inductor converters

3. Inverse of SEPIC

\[ M(D) = \frac{D}{1-D} \]

4. Buck

\[ M(D) = D^2 \]
6.3. Transformer isolation

Objectives:

- Isolation of input and output ground connections, to meet safety requirements
- Reduction of transformer size by incorporating high frequency isolation transformer inside converter
- Minimization of current and voltage stresses when a large step-up or step-down conversion ratio is needed — use transformer turns ratio
- Obtain multiple output voltages via multiple transformer secondary windings and multiple converter secondary circuits
A simple transformer model

**Multiple winding transformer**

\[ v_1(t) = n_1 i_1(t) + n_2 i_2(t) + n_3 i_3(t) \]

\[ v_2(t) = n_1 i_1'(t) + n_2 i_2'(t) + n_3 i_3'(t) \]

**Equivalent circuit model**

\[ v_1(t) = \frac{v_2(t)}{n_1} = \frac{v_3(t)}{n_2} = \frac{v_3'(t)}{n_3} = \ldots \]

\[ 0 = n_1 i_1'(t) + n_2 i_2'(t) + n_3 i_3'(t) + \ldots \]
The magnetizing inductance $L_M$

- Models magnetization of transformer core material
- Appears effectively in parallel with windings
- If all secondary windings are disconnected, then primary winding behaves as an inductor, equal to the magnetizing inductance
- At dc: magnetizing inductance tends to short-circuit. Transformers cannot pass dc voltages
- Transformer saturates when magnetizing current $i_M$ is too large
The magnetizing inductance is a real inductor, obeying

\[ v_1(t) = L_M \frac{d i_M(t)}{dt} \]

Integrate:

\[ i_M(t) - i_M(0) = \frac{1}{L_M} \int_0^t v_1(\tau)d\tau \]

Magnetizing current is determined by integral of the applied winding voltage. The magnetizing current and the winding currents are independent quantities. Volt-second balance applies: in steady-state, \( i_M(T_s) = i_M(0) \), and hence

\[ 0 = \frac{1}{T_s} \int_0^{T_s} v_1(t)dt \]
Transformer reset

- “Transformer reset” is the mechanism by which magnetizing inductance volt-second balance is obtained
- The need to reset the transformer volt-seconds to zero by the end of each switching period adds considerable complexity to converters
- To understand operation of transformer-isolated converters:
  - replace transformer by equivalent circuit model containing magnetizing inductance
  - analyze converter as usual, treating magnetizing inductance as any other inductor
  - apply volt-second balance to all converter inductors, including magnetizing inductance
6.3.1. Full-bridge and half-bridge isolated buck converters

**Full-bridge isolated buck converter**
Full-bridge, with transformer equivalent circuit

\[ V_s \]

\[ Q_1 \quad D_1 \quad Q_3 \quad D_3 \quad L \quad D_5 \]

\[ v_s(t) \quad i(t) \quad L_M \]

Ideal Transformer model

\[ Q_2 \quad D_2 \quad Q_4 \quad D_4 \]

\[ v(t) \quad C \quad R \]

\[ + \quad - \]
Full-bridge: waveforms

- During first switching period: transistors $Q_1$ and $Q_4$ conduct for time $DT_s$, applying volt-seconds $V_g DT_s$ to primary winding.

- During next switching period: transistors $Q_2$ and $Q_3$ conduct for time $DT_s$, applying volt-seconds $-V_g DT_s$ to primary winding.

- Transformer volt-second balance is obtained over two switching periods.

- Effect of nonidealities?
Effect of nonidealities on transformer volt-second balance

Volt-seconds applied to primary winding during first switching period:

\[(V_g - (Q_1 \text{ and } Q_4 \text{ forward voltage drops}))(Q_1 \text{ and } Q_4 \text{ conduction time})\]

Volt-seconds applied to primary winding during next switching period:

\[-(V_g - (Q_2 \text{ and } Q_3 \text{ forward voltage drops}))(Q_2 \text{ and } Q_3 \text{ conduction time})\]

These volt-seconds never add to exactly zero.

Net volt-seconds are applied to primary winding

Magnetizing current slowly increases in magnitude

Saturation can be prevented by placing a capacitor in series with primary, or by use of current programmed mode (Chapter 12)
Operation of secondary-side diodes

- During second ($D'$) subinterval, both secondary-side diodes conduct.
- Output filter inductor current divides approximately equally between diodes.
- Secondary amp-turns add to approximately zero.
- Essentially no net magnetization of transformer core by secondary winding currents.

Mathematical equations and diagrams illustrating the operation of secondary-side diodes in a converter circuit.
Volt-second balance on output filter inductor

\[ V = \langle v_s \rangle \]
\[ V = nDV_g \]
\[ M(D) = nD \quad \text{buck converter with turns ratio} \]
Half-bridge isolated buck converter

- Replace transistors $Q_3$ and $Q_4$ with large capacitors
- Voltage at capacitor centerpoint is $0.5V_g$
- $v_s(t)$ is reduced by a factor of two
- $M = 0.5 \, nD$
6.3.2. Forward converter

- Buck-derived transformer-isolated converter
- Single-transistor and two-transistor versions
- Maximum duty cycle is limited
- Transformer is reset while transistor is off
Forward converter
with transformer equivalent circuit
Forward converter: waveforms

- Magnetizing current, in conjunction with diode \( D_1 \), operates in discontinuous conduction mode
- Output filter inductor, in conjunction with diode \( D_3 \), may operate in either CCM or DCM
Subinterval 1: transistor conducts
Subinterval 2: transformer reset
Subinterval 3

\[ V_g \]

\[ i_M = 0 \]

\[ L_M \]

\[ v_1 \parallel v_2 \parallel v_3 \]

\[ i_1' \]

\[ i_1, i_2, i_3 \]

\[ Q_1 \text{ off} \quad D_1 \text{ off} \]

\[ D_3 \text{ on} \]

\[ v_{D3} \]

\[ C \]

\[ R \]

\[ V \]
Magnetizing inductance volt-second balance

\[ v_1 = D(V_g) + D_2 \left( -\frac{n_1}{n_2} V_g \right) + D_3(0) = 0 \]
Transformer reset

From magnetizing current volt-second balance:

\[ \langle v_1 \rangle = D \langle V_g \rangle + D_2 \left( -\frac{V_g n_1}{n_2} \right) + D_3(0) = 0 \]

Solve for \( D_2 \):

\[ D_2 = \frac{n_2}{n_1} D \]

\( D_3 \) cannot be negative. But \( D_3 = 1 - D - D_2 \). Hence

\[ D_3 = 1 - D - D_2 \geq 0 \]

\[ D_3 = 1 - D \left( 1 + \frac{n_2}{n_1} \right) \geq 0 \]

Solve for \( D \)

\[ D \leq \frac{1}{1 + \frac{n_2}{n_1}} \]

for \( n_1 = n_2 \):

\[ D \leq \frac{1}{2} \]
What happens when \( D > 0.5 \)

Magnetizing current waveforms, for \( n_1 = n_2 \)

\[
\begin{align*}
&\text{for } D < 0.5 \\
&\begin{array}{c}
\text{DT}_s \quad D_2 T_s \\ D_3 T_s
\end{array}
\end{align*}
\]

\[
\begin{align*}
&\text{for } D > 0.5 \\
&\begin{array}{c}
\text{DT}_s \quad D_2 T_s \\
2T_s
\end{array}
\end{align*}
\]
Conversion ratio $M(D)$

\[ \langle v_{D3} \rangle = V = \frac{n_3}{n_1}DV_g \]
Maximum duty cycle vs. transistor voltage stress

Maximum duty cycle limited to

\[ D \leq \frac{1}{1 + \frac{n_2}{n_1}} \]

which can be increased by increasing the turns ratio \( n_2 / n_1 \). But this increases the peak transistor voltage:

\[ \max(v_{Q1}) = V_g \left(1 + \frac{n_1}{n_2}\right) \]

For \( n_1 = n_2 \)

\[ D \leq \frac{1}{2} \quad \text{and} \quad \max(v_{Q1}) = 2V_g \]
The two-transistor forward converter

\[ V = nDV_g \quad D \leq \frac{1}{2} \quad \max(v_{Q1}) = \max(v_{Q2}) = V_g \]