6.2. A short list of converters

An infinite number of converters are possible, which contain switches embedded in a network of inductors and capacitors.

Two simple classes of converters are listed here:

- Single-input single-output converters containing a single inductor. The switching period is divided into two subintervals. This class contains eight converters.

- Single-input single-output converters containing two inductors. The switching period is divided into two subintervals. Several of the more interesting members of this class are listed.
Single-input single-output converters containing one inductor

- Use switches to connect inductor between source and load, in one manner during first subinterval and in another during second subinterval.
- There are a limited number of ways to do this, so all possible combinations can be found.
- After elimination of degenerate and redundant cases, eight converters are found:

  - *dc-dc converters*
    - buck
    - boost
    - buck-boost
    - noninverting buck-boost
  - *dc-ac converters*
    - bridge
    - Watkins-Johnson
  - *ac-dc converters*
    - current-fed bridge
    - inverse of Watkins-Johnson
Converters producing a unipolar output voltage

1. **Buck**

\[ M(D) = D \]

![Buck Converter Circuit]

2. **Boost**

\[ M(D) = \frac{1}{1-D} \]

![Boost Converter Circuit]
Converters producing a unipolar output voltage

3. **Buck-boost**

\[ M(D) = - \frac{D}{1-D} \]

4. **Noninverting buck-boost**

\[ M(D) = \frac{D}{1-D} \]
Converters producing a bipolar output voltage suitable as dc-ac inverters

5. Bridge

\[ M(D) = 2D - 1 \]

![Bridge circuit diagram]

6. Watkins-Johnson

\[ M(D) = \frac{2D - 1}{D} \]

or

![Watkins-Johnson circuit diagram]
Converters producing a bipolar output voltage suitable as ac-dc rectifiers

7. Current-fed bridge

\[ M(D) = \frac{1}{2D - 1} \]

8. Inverse of Watkins-Johnson

\[ M(D) = \frac{D}{2D - 1} \]
Several members of the class of two-inductor converters

1. Ĉuk

\[ M(D) = -\frac{D}{1 - D} \]

2. SEPIC

\[ M(D) = \frac{D}{1 - D} \]
Several members of the class of two-inductor converters

3. Inverse of SEPIC

\[ M(D) = \frac{D}{1-D} \]

4. Buck

\[ M(D) = D^2 \]
6.3. Transformer isolation

Objectives:

- Isolation of input and output ground connections, to meet safety requirements
- Reduction of transformer size by incorporating high frequency isolation transformer inside converter
- Minimization of current and voltage stresses when a large step-up or step-down conversion ratio is needed — use transformer turns ratio
- Obtain multiple output voltages via multiple transformer secondary windings and multiple converter secondary circuits
A simple transformer model

Multiple winding transformer

\[ v_1(t) \]
\[ n_1 : n_2 \]
\[ i_1(t) \]
\[ + \]
\[ i_2(t) \]
\[ + \]
\[ i_3(t) \]
\[ v_3(t) \]
\[ n_3 \]

Equivalent circuit model

\[ \frac{v_1(t)}{n_1} = \frac{v_2(t)}{n_2} = \frac{v_3(t)}{n_3} = \ldots \]
\[ 0 = n_1 i_1'(t) + n_2 i_2(t) + n_3 i_3(t) + \ldots \]
The magnetizing inductance $L_M$

- Models magnetization of transformer core material
- Appears effectively in parallel with windings
- If all secondary windings are disconnected, then primary winding behaves as an inductor, equal to the magnetizing inductance
- At dc: magnetizing inductance tends to short-circuit. Transformers cannot pass dc voltages
- Transformer saturates when magnetizing current $i_M$ is too large

Transformer core B-H characteristic:

- $B(t) \propto \int v_1(t) \, dt$
- $H(t) \propto i_M(t)$
- Slope $\propto L_M$
- Saturation
Volt-second balance in $L_M$

The magnetizing inductance is a real inductor, obeying

$$v_1(t) = L_M \frac{d i_M(t)}{dt}$$

integrate:

$$i_M(t) - i_M(0) = \frac{1}{L_M} \int_0^t v_1(\tau) d\tau$$

Magnetizing current is determined by integral of the applied winding voltage. The magnetizing current and the winding currents are independent quantities. Volt-second balance applies: in steady-state, $i_M(T_s) = i_M(0)$, and hence

$$0 = \frac{1}{T_s} \int_0^{T_s} v_1(t) dt$$
Transformer reset

- “Transformer reset” is the mechanism by which magnetizing inductance volt-second balance is obtained.
- The need to reset the transformer volt-seconds to zero by the end of each switching period adds considerable complexity to converters.
- To understand operation of transformer-isolated converters:
  - replace transformer by equivalent circuit model containing magnetizing inductance
  - analyze converter as usual, treating magnetizing inductance as any other inductor
  - apply volt-second balance to all converter inductors, including magnetizing inductance
6.3.1. Full-bridge and half-bridge isolated buck converters

**Full-bridge isolated buck converter**

[Diagram of full-bridge isolated buck converter]
Full-bridge, with transformer equivalent circuit
Full-bridge: waveforms

- During first switching period: transistors $Q_1$ and $Q_4$ conduct for time $DT_s$, applying volt-seconds $V_g DT_s$ to primary winding.

- During next switching period: transistors $Q_2$ and $Q_3$ conduct for time $DT_s$, applying volt-seconds $-V_g DT_s$ to primary winding.

- Transformer volt-second balance is obtained over two switching periods.

- Effect of nonidealities?
Effect of nonidealities on transformer volt-second balance

Volt-seconds applied to primary winding during first switching period:

\[(V_g - (Q_1 \text{ and } Q_4 \text{ forward voltage drops})) (Q_1 \text{ and } Q_4 \text{ conduction time})\]

Volt-seconds applied to primary winding during next switching period:

\[-(V_g - (Q_2 \text{ and } Q_3 \text{ forward voltage drops})) (Q_2 \text{ and } Q_3 \text{ conduction time})\]

These volt-seconds never add to exactly zero.

Net volt-seconds are applied to primary winding

Magnetizing current slowly increases in magnitude

Saturation can be prevented by placing a capacitor in series with primary, or by use of current programmed mode (Chapter 12)
Operation of secondary-side diodes

- During second ($D'$) subinterval, both secondary-side diodes conduct.
- Output filter inductor current divides approximately equally between diodes.
- Secondary amp-turns add to approximately zero.
- Essentially no net magnetization of transformer core by secondary winding currents.

![Diagram showing diagram and waveforms]
Volt-second balance on output filter inductor

\[ V = \langle v_s \rangle \]

\[ V = nDV_g \]

\[ M(D) = nD \quad \text{buck converter with turns ratio} \]
Half-bridge isolated buck converter

- Replace transistors $Q_3$ and $Q_4$ with large capacitors
- Voltage at capacitor centerpoint is $0.5V_g$
- $v_s(t)$ is reduced by a factor of two
- $M = 0.5 \, nD$
6.3.2. Forward converter

- Buck-derived transformer-isolated converter
- Single-transistor and two-transistor versions
- Maximum duty cycle is limited
- Transformer is reset while transistor is off
Forward converter
with transformer equivalent circuit
Forward converter: waveforms

- Magnetizing current, in conjunction with diode $D_1$, operates in discontinuous conduction mode
- Output filter inductor, in conjunction with diode $D_3$, may operate in either CCM or DCM
Subinterval 1: transistor conducts
Subinterval 2: transformer reset

\[ i_2 = i_M \frac{n_1}{n_2} \]

\[ Q_1 \text{ off} \]

\[ D_1 \text{ on} \]
Subinterval 3

\[ i_M = 0 \]
\[ L_M \]
\[ v_1 \]
\[ v_2 \]
\[ v_3 \]

\[ n_1 : n_2 : n_3 \]

\[ D_3 \text{ on} \]
\[ v_{D3} \]

\[ C \]
\[ R \]

\[ V \]

\[ Q_1 \text{ off} \]
\[ D_1 \text{ off} \]
Magnetizing inductance volt-second balance

\[ \langle v_1 \rangle = D(v_g) + D_2 \left( - \frac{V_g}{n_2} \right) + D_3(0) = 0 \]
Transformer reset

From magnetizing current volt-second balance:

\[ \langle v_1 \rangle = D(V_g) + D_2\left(-V_{g}n_1/n_2\right) + D_3(0) = 0 \]

Solve for \( D_2 \):

\[ D_2 = \frac{n_2}{n_1} D \]

\( D_3 \) cannot be negative. But \( D_3 = 1 - D - D_2 \). Hence

\[ D_3 = 1 - D - D_2 \geq 0 \]

\[ D_3 = 1 - D \left(1 + \frac{n_2}{n_1}\right) \geq 0 \]

Solve for \( D \)

\[ D \leq \frac{1}{1 + \frac{n_2}{n_1}} \quad \text{for } n_1 = n_2: \quad D \leq \frac{1}{2} \]
What happens when $D > 0.5$

magnetizing current waveforms, for $n_1 = n_2$

For $D < 0.5$:

- $i_M(t)$
- $DT_s$ to $D_2 T_s$ to $D_3 T_s$

For $D > 0.5$:

- $i_M(t)$
- $DT_s$ to $D_2 T_s$ to $2T_s$
Conversion ratio $M(D)$

\[
\langle v_{D3} \rangle = V = \frac{n_3}{n_1} DV_g
\]

Diagram showing the circuit components and their timing relations.
Maximum duty cycle vs. transistor voltage stress

Maximum duty cycle limited to

\[ D \leq \frac{1}{1 + \frac{n_2}{n_1}} \]

which can be increased by increasing the turns ratio \( n_2 / n_1 \). But this increases the peak transistor voltage:

\[ \max(v_{Q1}) = V_g \left( 1 + \frac{n_1}{n_2} \right) \]

For \( n_1 = n_2 \)

\[ D \leq \frac{1}{2} \quad \text{and} \quad \max(v_{Q1}) = 2V_g \]
The two-transistor forward converter

\[ V = nDV_g \]

\[ D \leq \frac{1}{2} \]

\[ \max(v_{Q1}) = \max(v_{Q2}) = V_g \]