Introduction to Power Electronics
ECEN 4797/5797

Lecture 17
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6.3.5. Boost-derived isolated converters

- A wide variety of boost-derived isolated dc-dc converters can be derived, by inversion of source and load of buck-derived isolated converters:
  - full-bridge and half-bridge isolated boost converters
  - inverse of forward converter: the “reverse” converter
  - push-pull boost-derived converter

Of these, the full-bridge and push-pull boost-derived isolated converters are the most popular, and are briefly discussed here.
Full-bridge transformer-isolated boost-derived converter

- Circuit topologies are equivalent to those of nonisolated boost converter
- With 1:1 turns ratio, inductor current $i(t)$ and output current $i_o(t)$ waveforms are identical to nonisolated boost converter
Transformer reset mechanism

- As in full-bridge buck topology, transformer volt-second balance is obtained over two switching periods.
- During first switching period: transistors $Q_1$ and $Q_4$ conduct for time $DT_s$, applying volt-seconds $VDT_s$ to secondary winding.
- During next switching period: transistors $Q_2$ and $Q_3$ conduct for time $DT_s$, applying volt-seconds $-VDT_s$ to secondary winding.

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Conducting devices: $Q_1, Q_2, Q_3, Q_4$
### Conversion ratio $M(D)$

#### Application of volt-second balance to inductor voltage waveform:

\[
\langle v_L \rangle = D(V_g) + D'(V_g - \frac{V}{n}) = 0
\]

Solve for $M(D)$:

\[
M(D) = \frac{V}{V_g} = \frac{n}{D'}
\]

—boost with turns ratio $n$
Push-pull boost-derived converter

\[ M(D) = \frac{V}{V_g} = \frac{n}{D'} \]
Push-pull converter based on Watkins-Johnson converter
6.3.6. Isolated versions of the SEPIC and Cuk converter

**Basic nonisolated SEPIC**

**Isolated SEPIC**
Isolated SEPIC

\[ M(D) = \frac{V}{V_g} = \frac{nD}{D'} \]
Inverse SEPIC

Nonisolated inverse SEPIC

Isolated inverse SEPIC
Obtaining isolation in the Cuk converter

Nonisolated Cuk converter

Split capacitor $C_1$ into series capacitors $C_{1a}$ and $C_{1b}$
Isolated Cuk converter

Insert transformer between capacitors $C_{1a}$ and $C_{1b}$

$$M(D) = \frac{V}{V_g} = \frac{nD}{D'}$$

Discussion

- Capacitors $C_{1a}$ and $C_{1b}$ ensure that no dc voltage is applied to transformer primary or secondary windings
- Transformer functions in conventional manner, with small magnetizing current and negligible energy storage within the magnetizing inductance
6.4. Converter evaluation and design

For a given application, which converter topology is best?

There is no ultimate converter, perfectly suited for all possible applications

Trade studies

- Rough designs of several converter topologies to meet the given specifications
- An unbiased quantitative comparison of worst-case transistor currents and voltages, transformer size, etc.

Comparison via switch stress, switch utilization, and semiconductor cost

Spreadsheet design
6.4.2. Converter design using computer spreadsheet

Given ranges of $V_g$ and $P_{load}$, as well as desired value of $V$ and other quantities such as switching frequency, ripple, etc., there are two basic engineering design tasks:

- Compare converter topologies and select the best for the given specifications
- Optimize the design of a given converter

A computer spreadsheet is a very useful tool for this job. The results of the steady-state converter analyses of Chapters 1-6 can be entered, and detailed design investigations can be quickly performed:

- Evaluation of worst-case stresses over a range of operating points
- Evaluation of design tradeoffs
Spreadsheet design example

**Specifications**

- Maximum input voltage $V_g$ 390 V
- Minimum input voltage $V_g$ 260 V
- Output voltage $V$ 15 V
- Maximum load power $P_{load}$ 200 W
- Minimum load power $P_{load}$ 20 W
- Switching frequency $f_s$ 100 kHz
- Maximum output ripple $\Delta v$ 0.1 V

- Input voltage: rectified 230 Vrms ±20%
- Regulated output of 15 V
- Rated load power 200 W
- Must operate at 10% load
- Select switching frequency of 100 kHz
- Output voltage ripple $\leq 0.1$ V

Compare single-transistor forward and flyback converters in this application

Specifications are entered at top of spreadsheet
Forward converter design, CCM

**Design variables**
- Reset winding turns ratio $n_2/n_1$: 1
- Turns ratio $n_3/n_1$: 0.125
- Inductor current ripple $\Delta i$: 2A ref to sec

- Design for CCM at full load; may operate in DCM at light load
Flyback converter design, CCM

**Design variables**
- Turns ratio $n_2/n_1$ 0.125
- Inductor current ripple $\Delta i$ 3 A ref to sec

- Design for CCM at full load; may operate in DCM at light load
Enter results of converter analysis into spreadsheet
(Forward converter example)

Maximum duty cycle occurs at minimum $V_g$ and maximum $P_{load}$.
Converter then operates in CCM, with

$$D = \frac{n_1}{n_3} \frac{V}{V_g}$$

Inductor current ripple is

$$\Delta i = \frac{D'VT_s}{2L}$$

Solve for $L$:

$$L = \frac{D'VT_s}{2\Delta i}$$

$\Delta i$ is a design variable. For a given $\Delta i$, the equation above can be used to determine $L$. To ensure CCM operation at full load, $\Delta i$ should be less than the full-load output current. $C$ can be found in a similar manner.
Forward converter example, continued

Check for DCM at light load. The solution of the buck converter operating in DCM is

\[ V = \frac{n_3}{n_1} V_g \frac{2}{\sqrt{1 + \frac{4K}{D^2}}} \]

with \( K = \frac{2L}{RT_s} \) and \( R = \frac{V^2}{P_{\text{load}}} \)

These equations apply equally well to the forward converter, provided that all quantities are referred to the transformer secondary side.

Solve for \( D \):

\[ D = \frac{2\sqrt{K}}{\sqrt{\left( \frac{2n_3 V_g}{n_1 V} - 1 \right)^2 - 1}} \text{ in DCM} \]

\[ D = \frac{n_1 V}{n_3 V_g} \text{ in CCM} \]

at a given operating point, the actual duty cycle is the small of the values calculated by the CCM and DCM equations above. Minimum \( D \) occurs at minimum \( P_{\text{load}} \) and maximum \( V_g \).
More regarding forward converter example

Worst-case component stresses can now be evaluated.

Peak transistor voltage is

$$\max(v_{Q1}) = V_g \left( 1 + \frac{n_1}{n_2} \right)$$

RMS transistor current is

$$I_{Q1,rms} = \frac{n_3}{n_1} \sqrt{D} \sqrt{I^2 + \frac{(\Delta i)^2}{3}} \approx \frac{n_3}{n_1} \sqrt{D} I$$

(this neglects transformer magnetizing current)

Other component stresses can be found in a similar manner. Magnetics design is left for a later chapter.
### Results: forward and flyback converter spreadsheets

#### Forward converter design, CCM

<table>
<thead>
<tr>
<th>Design variables</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset winding turns ratio ( n_2/n_1 )</td>
<td>1</td>
</tr>
<tr>
<td>Turns ratio ( n_3/n_1 )</td>
<td>0.125</td>
</tr>
<tr>
<td>Inductor current ripple ( \Delta i )</td>
<td>2 A ref to sec</td>
</tr>
</tbody>
</table>

#### Flyback converter design, CCM

<table>
<thead>
<tr>
<th>Design variables</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Turns ratio ( n_2/n_1 )</td>
<td>0.125</td>
</tr>
<tr>
<td>Inductor current ripple ( \Delta i )</td>
<td>3 A ref to sec</td>
</tr>
</tbody>
</table>

#### Results

<table>
<thead>
<tr>
<th></th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum duty cycle ( D )</td>
<td>0.462</td>
</tr>
<tr>
<td>Minimum ( D ), at full load</td>
<td>0.308</td>
</tr>
<tr>
<td>Minimum ( D ), at minimum load</td>
<td>0.251</td>
</tr>
</tbody>
</table>

#### Worst-case stresses

<table>
<thead>
<tr>
<th></th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak transistor voltage ( v_{Q1} )</td>
<td>780 V</td>
</tr>
<tr>
<td>Rms transistor current ( i_{Q1} )</td>
<td>1.13 A</td>
</tr>
<tr>
<td>Transistor utilization ( U )</td>
<td>0.226</td>
</tr>
<tr>
<td>Peak diode voltage ( v_{D2} )</td>
<td>49 V</td>
</tr>
<tr>
<td>Rms diode current ( i_{D2} )</td>
<td>9.1 A</td>
</tr>
<tr>
<td>Peak diode voltage ( v_{D3} )</td>
<td>49 V</td>
</tr>
<tr>
<td>Rms diode current ( i_{D3} )</td>
<td>11.1 A</td>
</tr>
<tr>
<td>Rms output capacitor current ( i_C )</td>
<td>1.15 A</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak transistor voltage ( v_{Q1} )</td>
<td>510 V</td>
</tr>
<tr>
<td>Rms transistor current ( i_{Q1} )</td>
<td>1.38 A</td>
</tr>
<tr>
<td>Transistor utilization ( U )</td>
<td>0.284</td>
</tr>
<tr>
<td>Peak diode voltage ( v_{D1} )</td>
<td>64 V</td>
</tr>
<tr>
<td>Rms diode current ( i_{D1} )</td>
<td>16.3 A</td>
</tr>
<tr>
<td>Peak diode current ( i_{D1} )</td>
<td>22.2 A</td>
</tr>
<tr>
<td>Rms output capacitor current ( i_C )</td>
<td>9.1 A</td>
</tr>
</tbody>
</table>
Discussion: transistor voltage

*Flyback converter*

Ideal peak transistor voltage: 510V

Actual peak voltage will be higher, due to ringing causes by transformer leakage inductance

An 800V or 1000V MOSFET would have an adequate design margin

*Forward converter*

Ideal peak transistor voltage: 780V, 53% greater than flyback

Few MOSFETs having voltage rating of over 1000 V are available —when ringing due to transformer leakage inductance is accounted for, this design will have an inadequate design margin

Fix: use two-transistor forward converter, or change reset winding turns ratio

A conclusion: reset mechanism of flyback is superior to forward
Discussion: rms transistor current

**Forward**

- 1.13A worst-case
- Transistor utilization 0.226

**Flyback**

- 1.38A worst case, 22% higher than forward
- Transistor utilization 0.284

CCM flyback exhibits higher peak and rms currents. Currents in DCM flyback are even higher
Discussion: secondary-side diode and capacitor stresses

Forward

- peak diode voltage 49V
- rms diode current 9.1A / 11.1A
- rms capacitor current 1.15A

Flyback

- peak diode voltage 64V
- rms diode current 16.3A
- peak diode current 22.2A
- rms capacitor current 9.1A

Secondary-side currents, especially capacitor currents, limit the practical application of the flyback converter to situations where the load current is not too great.
Part II
Converter Dynamics and Control

7. AC equivalent circuit modeling
8. Converter transfer functions
9. Controller design
10. Ac and dc equivalent circuit modeling of the discontinuous conduction mode
11. Current programmed control
Chapter 7. AC Equivalent Circuit Modeling

7.1. Introduction
7.2. The basic ac modeling approach
7.3. Example: A nonideal flyback converter
7.4. State-space averaging
7.5. Circuit averaging and averaged switch modeling
7.6. The canonical circuit model
7.7. Modeling the pulse-width modulator
7.8. Summary of key points
7.1. Introduction

Objective: maintain $v(t)$ equal to an accurate, constant value $V$.

There are disturbances:
- in $v_g(t)$
- in $R$

There are uncertainties:
- in element values
- in $V_g$
- in $R$

A simple dc-dc regulator system, employing a buck converter
Applications of control in power electronics

**Dc-dc converters**

Regulate dc output voltage.

Control the duty cycle \( d(t) \) such that \( v(t) \) accurately follows a reference signal \( v_{\text{ref}} \).

**Dc-ac inverters**

Regulate an ac output voltage.

Control the duty cycle \( d(t) \) such that \( v(t) \) accurately follows a reference signal \( v_{\text{ref}}(t) \).

**Ac-dc rectifiers**

Regulate the dc output voltage.

Regulate the ac input current waveform.

Control the duty cycle \( d(t) \) such that \( i_g(t) \) accurately follows a reference signal \( i_{\text{ref}}(t) \), and \( v(t) \) accurately follows a reference signal \( v_{\text{ref}} \).
Objective of Part II

Develop tools for modeling, analysis, and design of converter control systems

Need dynamic models of converters:

How do ac variations in $v_g(t)$, $R$, or $d(t)$ affect the output voltage $v(t)$?

What are the small-signal transfer functions of the converter?

• Extend the steady-state converter models of Chapters 2 and 3, to include CCM converter dynamics (Chapter 7)
• Construct converter small-signal transfer functions (Chapter 8)
• Design converter control systems (Chapter 9)
• Model converters operating in DCM (Chapter 10)
• Current-programmed control of converters (Chapter 11)
Modeling

- Representation of physical behavior by mathematical means
- Model dominant behavior of system, ignore other insignificant phenomena
- Simplified model yields physical insight, allowing engineer to design system to operate in specified manner
- Approximations neglect small but complicating phenomena
- After basic insight has been gained, model can be refined (if it is judged worthwhile to expend the engineering effort to do so), to account for some of the previously neglected phenomena
Neglecting the switching ripple

Suppose the duty cycle is modulated sinusoidally:

\[ d(t) = D + D_m \cos \omega_m t \]

where \( D \) and \( D_m \) are constants, \( |D_m| << D \), and the modulation frequency \( \omega_m \) is much smaller than the converter switching frequency \( \omega_s = 2\pi f_s \).

The resulting variations in transistor gate drive signal and converter output voltage:

![Gate drive signal and converter output voltage](image-url)
Output voltage spectrum
with sinusoidal modulation of duty cycle

Contains frequency components at:
- Modulation frequency and its harmonics
- Switching frequency and its harmonics
- Sidebands of switching frequency

With small switching ripple, high-frequency components (switching harmonics and sidebands) are small.

If ripple is neglected, then only low-frequency components (modulation frequency and harmonics) remain.
Objective of ac converter modeling

- Predict how low-frequency variations in duty cycle induce low-frequency variations in the converter voltages and currents
- Ignore the switching ripple
- Ignore complicated switching harmonics and sidebands

Approach:
- Remove switching harmonics by averaging all waveforms over one switching period
Averaging to remove switching ripple

Average over one switching period to remove switching ripple:

\[ L \frac{d\langle i_L(t) \rangle_{T_s}}{dt} = \langle v_L(t) \rangle_{T_s} \]

\[ C \frac{d\langle v_C(t) \rangle_{T_s}}{dt} = \langle i_C(t) \rangle_{T_s} \]

where

\[ \langle x_L(t) \rangle_{T_s} = \frac{1}{T_s} \int_{t}^{t+T_s} x(\tau) \, d\tau \]

Note that, in steady-state,

\[ \langle v_L(t) \rangle_{T_s} = 0 \]
\[ \langle i_C(t) \rangle_{T_s} = 0 \]

by inductor volt-second balance and capacitor charge balance.
Nonlinear averaged equations

The averaged voltages and currents are, in general, nonlinear functions of the converter duty cycle, voltages, and currents. Hence, the averaged equations

\[ L \frac{d}{dt} \langle i_L(t) \rangle_{T_s} = \langle v_L(t) \rangle_{T_s} \]

\[ C \frac{d}{dt} \langle v_C(t) \rangle_{T_s} = \langle i_C(t) \rangle_{T_s} \]

constitute a system of nonlinear differential equations.

Hence, must linearize by constructing a small-signal converter model.
Small-signal modeling of the BJT

Nonlinear Ebers-Moll model

Linearized small-signal model, active region
Buck-boost converter: nonlinear static control-to-output characteristic

Example: linearization at the quiescent operating point

\[ D = 0.5 \]
Result of averaged small-signal ac modeling

Small-signal ac equivalent circuit model

\[ + \quad V_g(t) - V_d(t) + \quad \]

\[ \frac{1}{D} \quad I \hat{d}(t) \quad \frac{1}{D'} \quad \hat{d}(t) \quad \]

\[ L \quad \quad \quad \]

\[ + \quad \frac{1}{R} \quad \hat{v}(t) \quad \]

\[ \hat{v}_g(t) \quad I \hat{d}(t) \quad \]

buck-boost example