Modeling and Control of Power Electronics Systems

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Lecture 41
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Introduction to Inverters

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Single-Phase Inverter Approaches
The Solar Application
Single-Phase Solar Inverters
Microinverters
A Basic Single-Phase Inverter Circuit

- $L$-$C$ filter may or may not be present
- Simple resistive load illustrated; actual AC loads are more complex
- Even in the single-phase case, there are multiple ways to control the switches
- Applications:
  - Uninterruptable power supply (UPS)
  - AC motor drive
  - Fluorescent lamp driver
  - Solar power inverter
  - Automobile AC power inverter

Some three-phase applications:
- AC motor drives
- Inverters for wind and solar
- Electric vehicles
- DC transmission line stations
The “Modified Sine Wave” Inverter

H-bridge switches at the output frequency
- Waveform is highly nonsinusoidal, with significant harmonics
- Some ac loads can tolerate this waveform, others cannot
- Inexpensive, efficient

Control of ac rms voltage by control of duty cycle $D$:

$$V_{ac,RMS} = \sqrt{\frac{1}{T} \int_0^T v_{ac}^2(t) \, dt} = \sqrt{D} \cdot V_{HVDC}$$

Standalone inverter: inverter drives a passive load, and regulates the voltage supplied to the load
The “True Sine Wave” Inverter

Use of PWM with high frequency switching to produce a sinusoidal ac voltage having low harmonic content. Typically an L-C filter is included to meet EMI requirements.

Two-level waveform

Three-level waveform

- Switches 1a and 1b are driven by the same gate drive signal, and conduct during $d$ interval.
- Switches 2a and 2b are driven by the complement and conduct during $d'$ interval.

$v(t) = (2d(t) - 1) V_g$

- For positive half cycle, switch 1b is on. Switches 1a and 2a operate with PWM.
- For negative half cycle, switch 2a is on. Switches 2b and 1b operate with PWM.

$v(t) = \pm d(t) V_g$

Alternate: b switches switch at the line frequency, and a switches operate with PWM.
- Three-level exhibits reduced switching loss.
Standalone vs. grid-tied applications

**Standalone inverter:**
Inverter regulates ac voltage

- Inverter
  - $V_{dc}$
  - $d_{inv}$
  - $v_{ac}(t)$
  - PWM
  - $G_{v3}(s)$
  - $v_{ref}(t)$
  - Sinusoidal reference

- AC load

**Grid-tied inverter:**
Inverter regulates its ac current

- Inverter
  - $V_{dc}$
  - $d_{inv}$
  - $i_{ac}(t)$
  - PWM
  - $G_{v3}(s)$
  - $i_{ref}(t)$
  - Phase-locked loop
  - Sinusoidal unit amplitude

- AC load
  - $v_{ac}(t)$
Reactive power

For a standalone application, the inverter must be capable of supplying whatever current waveform is demanded by the ac load

- Reactive load, in which current is phase-shifted relative to voltage
- Distorted current

In most grid-tied applications, the inverter supplies a low-THD current waveform to the grid, with power factor very close to unity.

- Improved efficiency
- This opens the possibility of simpler converter topologies using single-quadrant switches
The grid-tied solar inverter application

- AC voltage is determined by the utility system (“infinite bus”)
- Power is determined by the solar array
- Inverter produces ac current synchronized to the utility, with amplitude dependent on array power
Functions performed by the inverter

**Maximum power point tracking:** operate the solar array at the voltage that maximizes generated power

**120 Hz energy storage:** the difference between the constant power supplied by the array and the 120 Hz pulsating power flowing into the utility is supplied/stored in the capacitor

**AC current control:** ac line current must meet harmonic requirements (THD < 5%), with unity power factor

- Array voltage, capacitor voltage, and ac line voltage are independent
- System resembles PWM rectifier system, but with power flow reversed
An Inverter System

DC-DC

v_{bus}(t)

Inverter

EMI

v_{ac}(t)

v_{pv}(t)

PV

DC-DC

PWM

H_1

G_{c3}(s)

MPPT

V_{ref-pv}

H_2

G_{c2}(s)

V_{ref-bus}

H_3

G_{c3}(s)

PWM

\frac{d}{dt} \times i_{bus}

i_{bus}

\frac{d}{dt} \times v_{bus}(t)

v_{bus}(t)

\frac{d}{dt} \times i_{ac}(t)

i_{ac}(t)

\frac{d}{dt} \times v_{ac}(t)

v_{ac}(t)

sinusoid unit amplitude phase-locked to v_{ac}

Phase-locked loop
Standards

IEEE 1547: standard for connecting a renewable energy source to the utility grid
  • Current harmonic limit (THD < 5%)
  • Anti-islanding (detect loss of grid, shut down within 1 sec)
  • Disconnection when grid frequency or grid voltage is out of bounds

National Electric Code
UL 1741

Weighted Efficiency standards: California Energy Commission (CEC)

| Power level, % of rated | Weight | • Provides a way to compare products of different companies
|------------------------|--------|• Weightings reflect typical distribution of array power experienced in California |
| 100%                   | 0.05   | |
| 75%                    | 0.53   | |
| 50%                    | 0.21   | |
| 30%                    | 0.12   | |
| 20%                    | 0.05   | |
| 10%                    | 0.04   | |
Microinverters

One inverter per panel

- Mounted on or near the panel—on roof
- MPPT on per-panel basis
- Conventional AC wiring reduces Balance-of-system cost
- Straightforward expandability
- Reliability? Efficiency? Rated temperature?

Ascension Tech. microinverter, 1998

Enphase microinverter, 2008
Elements of a Microinverter System

Microinverter power train:
- DC-DC converter (high boost ratio)
- Energy storage capacitor
- Inverter

Rooftop system
- Microinverters include most or all of grid interface control
- Central box
Microinverter Approaches

II. VARIABLE FREQUENCY PEAK CURRENT CONTROLLER

In this section we present the constant peak current switching scheme. This new scheme is derived through an analysis of weighted losses in BCM, an analysis that demonstrates that the dominant loss for BCM is switching loss.

To improve the weighted efficiency, we explore which peak current is optimal at each output power, and show that in DCM the optimal peak current is constant.

A common topology for micro-inverters is the two-stage topology [22], [23], which includes a boost stage and an inverter stage, as shown in Fig. 1. Typically the boost stage tracks the maximum power point of the PV source, and boosts the low PV input voltage to a higher voltage. The inverter stage generates the AC current that is injected to the AC line.

Despite various new topologies that have been demonstrated in recent literature [5], the typical low-cost micro-inverter is still designed either as a full-bridge stage, or as a buck stage with an unfolder stage. The unfolder stage, if present, switches at the zero-crossings of the line voltage to convert the rectified sinusoid at the buck output to a full sinusoid on the AC line.

An illustration of the Boundar y Conduction Mode (BCM) waveform is shown in Fig. 2. Although it is soft-switching, and operates with low RMS current, a disadvantage of BCM is its high average switching frequency, which causes high switching losses. As demonstrated by equation (1), the BCM waveform has the highest switching frequency among all DCM waveforms. This is because the peak current of BCM is equal to \( i_{pk}(t) = 2i_{out}(t) \), which is the H-bridge inverter.

- **H-bridge inverter**
- **Buck converter plus unfolder**

*Unfolder*: similar to bridge rectifier, but power flows in reverse direction. Implemented using transistors that switch at ac line frequency.
Inverter sinewave synthesis approaches

We can employ any of the approaches we have already discussed for PWM rectifier systems:

- Average current control
- Peak current control
- Boundary conduction mode
- Hysteretic control
- Discontinuous conduction mode control
- Cycle-by-cycle control

(and there are a few we didn’t discuss, most notably harmonic elimination, that could be employed for either rectifiers or inverters)
Sythesizing a Sinusoidal Current: Boundary Conduction Mode (BCM)

Inductor current waveform, BCM

Loss components at different solar irradiance levels, BCM (300 W, 240 Vac example)
Discontinuous conduction mode (DCM)

- Higher conduction loss
- Lower switching loss
- A net improvement in CEC efficiency

Weighted efficiency vs. inductor size, DCM vs. BCM
300 W, 240 Vac example
Measured Results: 300 W Microinverter Prototype

The current sense resistor is located between the FET source and ground, and senses the rising slope of the inductor current. The only function of this sensed signal is to turn off the FET when the inductor current reaches the designated peak current $I_{pk}$. The voltage sensor is implemented by a comparator that connects to an auxiliary winding (3 turns) on the inductor. Its purpose is to detect the moment in which the inductor current reaches zero, the moment in which the cycle-by-cycle integrator voltage starts to discharge (See Fig. 8). As explained in Section IV, at this moment the switching node voltage starts oscillating, and the voltage across the inductor changes polarity. This change is detected by the comparator, which resets the controller SR-flip-flop. The oscillating output of the auxiliary winding comparator is shown in Fig. 12 (blue waveform). This graph also shows the voltage across the cycle-by-cycle integration capacitor ($v_{int}$, yellow waveform). The inverter waveforms over a 60 Hz line cycle are shown in Fig. 13.

Fig. 12. Inverter waveforms at a DC operating point. Ch1 (yellow) cycle-by-cycle integration capacitor voltage $v_{int}(t)$, Ch2 (blue) auxiliary winding voltage sensor, at comparator output, Ch4 (green) inductor current $i_L(t)$. Conditions: $V_{dc} = 426.8$ V, $I_{dc} = 0.98$ A, $v_{out} = 330.1$ V, $i_{out} = 1.259$ A.

Fig. 13. Inverter waveforms over a line cycle. Ch1 (yellow) AC line voltage sensor, Ch2 (blue) AC current $i_{ac}(t)$, Ch3 (magenta) reference signal $i_{ref}(t)$, Ch4 (green) inductor current $i_L(t)$. Conditions: $V_{dc} = 425$ V, $I_{dc} = 0.462$ A, $R_{load} = 253 \Omega$.

The efficiency of the inverter is measured at static DC operating points. These tests are done with a power supply at the input and a variable load resistor ($R_{load}$) at the output. To increase the accuracy of the measurements, the meters at the input and output are filtered by large EMI inductors. The efficiency results are shown in Fig. 14. The various curves in the figure correspond to tests with different average AC powers ($P_{ac}$). At each such test the load resistor is set to $R_{load} = \frac{V_{dc}^2}{P_{ac}}$, and the instantaneous output power is scanned in the range 0 … 2 $P_{ac}$.

Fig. 14. Efficiency measurements at DC operating points, for various average AC powers.

At each power level, the AC efficiency is computed by averaging the DC efficiencies over a line cycle. The results are again averaged by the CEC weighted average formula to obtain the overall CEC efficiency. The AC efficiency is computed by equation (9), and the results are summarized in Table II.

$$
\eta_{AC} = \frac{\int_0^{2P_{ac}} p_{out}(t) dt}{\int_0^{2P_{ac}} P_{ac} dt}
$$

In this equation, $P_{ac}$ is the average AC power, $p_{out}(t)$ is the output power at a DC operating point, and $\eta_{DC}(p_{out})$ is the efficiency at those operating points, as shown in Fig. 14. The weighted CEC efficiency is found to be 99.15 %.

<table>
<thead>
<tr>
<th>CEC power level</th>
<th>weight</th>
<th>average AC power $P_{ac}$</th>
<th>Average loss over AC cycle</th>
<th>average AC efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 %</td>
<td>0.05</td>
<td>300 W</td>
<td>2.6 W</td>
<td>99.13 %</td>
</tr>
<tr>
<td>75 %</td>
<td>0.53</td>
<td>225 W</td>
<td>1.97 W</td>
<td>99.12 %</td>
</tr>
<tr>
<td>50 %</td>
<td>0.21</td>
<td>150 W</td>
<td>1.26 W</td>
<td>99.16 %</td>
</tr>
<tr>
<td>30 %</td>
<td>0.12</td>
<td>90 W</td>
<td>0.7 W</td>
<td>99.22 %</td>
</tr>
<tr>
<td>20 %</td>
<td>0.05</td>
<td>60 W</td>
<td>0.45 W</td>
<td>99.24 %</td>
</tr>
<tr>
<td>10 %</td>
<td>0.04</td>
<td>30 W</td>
<td>0.24 W</td>
<td>99.2 %</td>
</tr>
</tbody>
</table>

| Overall weighted CEC efficiency = 99.15 % |
Development of Electrical Model of the Photovoltaic Cell, slide 1

**Photogeneration**
Semiconductor material absorbs photons and converts into hole-electron pairs if
- Photon energy $h\nu > E_{\text{gap}}$ (*)
- Energy in excess of $E_{\text{gap}}$ is converted to heat
- Photo-generated current $I_0$ is proportional to number of absorbed photons satisfying (*)

**Charge separation**
Electric field created by diode structure separates holes and electrons
Open circuit voltage $V_{oc}$ depends on diode characteristic, $V_{oc} < E_{\text{gap}}/q$
Current source $I_0$ models photo-generated current

$I_0$ is proportional to the *solar irradiance*, also called the "*insolation*":

$$I_0 = k \text{(solar irradiance)}$$

Solar irradiance is measured in W/m$^2$
Diode models $p$–$n$ junction

Diode $i$–$v$ characteristic follows classical exponential diode equation:

$$I_d = I_{dss} (e^{\frac{V_d}{V_a}} - 1)$$

The diode current $I_d$ causes the terminal current $I_{pv}$ to be less than or equal to the photo-generated current $I_0$. 
Modeling nonidealities:

- $R_1$: defects and other leakage current mechanisms
- $R_2$: contact resistance and other series resistances
Cell characteristic

Cell output power is $P_{pv} = I_{pv} V_{pv}$

At the maximum power point (MPP):

\[ V_{pv} = V_{mp} \]
\[ I_{pv} = I_{mp} \]

At the short circuit point:

\[ I_{pv} = I_{sc} = I_0 \]
\[ P_{pv} = 0 \]

At the open circuit point:

\[ V_{pv} = V_{oc} \]
\[ P_{pv} = 0 \]
Maximum Power Point Tracking

Automatically operate the PV panel at its maximum power point

Some possible MPPT algorithms:

• Perturb and observe
• Periodic scan
• Newton’s method, or related hill-climbing algorithms
• What is the control variable? Where is the power measured?

$I-V$ curve with partial shading

Power vs. voltage
Example MPPT: Perturb and Observe

• A well-known approach
• Works well if properly tuned
• When not well tuned, maximum power point tracker (MPPT) is slow and can get confused by rapid changes in operating point
• A common choice: “control” is switch duty cycle

**Basic algorithm**

Measure power
Loop:
• Perturb the operating point in some direction
• Wait for system to settle
• Measure power
• Did the power increase?
  Yes: retain direction for next perturbation
  N: reverse direction for next perturbation

Repeat
Control Issues:
MPPT by Perturb-and-Observe

Key elements of digital controller

- Find PV voltage that maximizes power output
- Switching converter is high noise environment
- This “noise” is partly correlated to the control, and hence isn’t entirely random
- The highly-filtered dc control characteristic exhibits many small peaks (“traps”), where P&O algorithm gets stuck
- More noise makes P&O work better!
Typical experimental data

- Perturb-and-observe step time of 15 msec
- Perturb-and-observe algorithm may take minutes to find max power
- Weather can change in seconds
- Improved algorithm achieves max power in seconds
- Adaptive algorithm finds max power quickly, then reduces jitter size to improve equilibrium MPPT accuracy