

Fig 7.48 (d) (single power supply)

(d)

\[ V_{SG} \]

\[ V_{PD} \]

\[ R_{SG} \]

\[ R_{G1} \]

\[ C_{CI} \]

\[ R_{G2} \]

\[ R_{D} \]

\[ R_{S} \]

> \( V_{G} \) fixed by voltage divider

> \( R_{G1,2} \) large w/o affecting \( I_{D} \) since \( I_{G} = 0 \)

> large \( R_{G} \) \( \Rightarrow \) large input resistance needed for min signal attenuation

Ex 7.11

Design 7.48 (c) for DC drain current

\[ I_{D} = 0.5 \text{ mA} \]

\[ V_{T} = 1V \]

\[ k_{n} = 1 \text{ mA/\( \sqrt{2} \)} \]

\[ \lambda = 0 \]

\[ V_{PD} = 15 \text{ V} \]

\[ \text{Calculate } \% \text{ change in } I_{D} \text{ when MOSFET replaced with another transistor with } V_{T} = 1.5 \text{ V but same other parameters} \]
Part I: Rule of Thumb

RD and RS chosen to provide 1/3 of VDD across RD, RS and transistor

\[ V_D = 10V, \quad V_S = 5V \]

\[ R_D = \frac{V_{DD} - V_D}{I_D} = \frac{15V - 10V}{0.5mA} = 10k\Omega \]

\[ R_S = \frac{V_S}{I_D} = \frac{5V}{0.5mA} = 10k\Omega \]

\[ I_D = \frac{1}{2} \ln \left( \frac{W}{L} \right) V_{DD}^2 \]

\[ 0.5mA = \frac{1}{2} \left( 1mA/V^2 \right) V_{DD}^2 \Rightarrow V_{DD} = 1V \]

\[ V_{GS} = V_T + V_{OV} = 1 + 1 = 2V \]

Since \( V_S = 5V \)

\[ V_G = V_S + V_{GS} = 5V + 2V = 7V \]

Select \( R_{G1} = 8 \, \text{M} \Omega \) and \( R_{G2} = 7 \, \text{M} \Omega \)

DC voltage at drain allows for signals of \( +5V \) (VDD) and \( -4V \) (V_G - V_D)

Part II: Replace Transistor with one with \( V_T = 0.5V \)

(A) \( 0.5mA = I_D = \frac{1}{2} \left( 1mA/V^2 \right) (V_{GS} - 15V)^2 \)

(B) \[ V_G = V_{GS} + I_D R_S \]

\[ 7 = V_{GS} + 10 I_D \]

Solve (A) + (B) \( \Rightarrow I_D = 0.455mA \)

\[ \Delta I_D / I_D = \frac{(0.455 - 0.5)mA}{0.5mA} = -9\% \]
7.4.1 Biasing using D\rightarrow G feedback resistor

Fig 7.50

\[ V_{DD} - I_G = 0 \Rightarrow V_G = V_D \]

\[ R_D \quad - \quad V_{GS} = V_{DS} = V_{DD} - I_D R_D \]

ID stabilized

- Large RG \Rightarrow large input for common source amplifier

Bias with constant current source

7.5 Discrete circuit amplifiers

Common source (Fig 5.57, etched)
Common source voltage on gate, $V_o$ on drain

Draw small signal model

\[ R_{\text{in}} = \frac{V_i}{i_i} \implies i_i = \frac{V_i}{R_G} \implies R_{\text{in}} = R_G \]

\[ R_0 = \frac{V_x}{i_x} \mid V_i = 0 \implies V_i = 0 \implies V_{gs} = 0 \implies GmV_{gs} = 0 \]

\[ R_0 = R_0 || R_D \]

Voltage gain

\[ A_v = -Gm (R_0 || R_D || R_L) = \frac{V_o}{V_i} \]

\[ A_v = A_v \left( \frac{R_L}{R_L + R_0} \right) \]

\[ A_v = \frac{V_o}{V_i} \mid R_L = \infty = -Gm (R_0 || R_D) \]

Usually, $R_0 > R_D \implies R_0$ decreases $A_v$ slightly and increases $R_0$

Overall voltage gain

\[ G_v = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} \]

\[ A_v = \left( \frac{-R_G}{R_{\text{sig}} + R_G} \right) Gm (R_0 || R_D || R_L) \]
CS amplifier with source resistance

(Ref 5.58, 4th ed)

> Find $R_{in}/R_o/A_{vol}/A_v$

> Draw small signal model (neglect $R_o$)

Unlike CS amplifier, $V_i \neq V_{gs}$

$$V_{gs} = V_i \frac{1/gm}{1/gm + R_s}$$

> $R_s$ controls $V_{gs}$ to be sufficiently small for small signal operation - avoid nonlinear distortion
Rs provides negative feedback but reduces voltage gain

\[ i_d = i_s = Vgs \cdot g_m = \frac{g_m V_i}{1 + g_m R_s} \]

\( i_d \) is reduced by \( \frac{1}{1 + g_m R_s} \)

\[ V_o = -i_d (R_D || R_L) = -\frac{g_m (R_D || R_L) V_i}{1 + g_m R_s} \]

\[ G_v = \left( \frac{R_g}{R_g + R_{sig}} \right) A_v \]

Compared with CS amplifier, \( A_v / A_{v0} / G_v \) are all reduced by \( \frac{1}{1 + g_m R_s} \)

**Common Gate amplifier** (6th ed, Fig 5.59(a))

- Gate grounded
- Signal fed into source
- Output is drain
Draw small signal model with $R_o$

\[ R_{in} = \frac{V_i}{I_i} \quad I_i = \frac{V_i}{1/gm} \quad \Rightarrow \quad R_{in} = \frac{1}{gm} \]

\[ R_o = \frac{V_x}{I_x} \quad |V_i = 0 = R_D \quad \Rightarrow \quad R_o = R_D \]

Typical

\[ G_m \approx 1 \text{ m}\Lambda/V \quad R_{in} \approx 1 \text{k}\Omega \]

Can cause significant signal attenuation

\[ V_i = U_{syg} \left( \frac{R_{in}}{R_{in} + R_{syg}} \right) = U_{syg} \left( \frac{1}{1 + gmR_{syg}} \right) \]

\[ R_{syg} \ll \frac{1}{gm} \text{ needed} \]

\[ I_i = \frac{V_i}{R_{in}} = G_m V_i \]

\[ I = -I_i = -G_m V_i \]

\[ V_0 = -I_D (R_D || R_L) = G_m V_i \cdot (R_D || R_L) \]
\[ A_{v} = g_{m} (R_D || R_L) \]
\[ A_{v0} \uparrow R_L = \infty = g_{m} R_D \]

\[
G_V = \frac{R_I}{R_I + R_{sy}} \quad A_V = \frac{A_V}{1 + g_{m} R_{sy}}
\]

Compared with CS amplifier:

1. CS amplifier inverting
   CG amplifier non-inverting

2. CS high Rin
   CG low Rin

3. \( A_V \) almost same
   \( G_V \) reduced by \( (1 + g_{m} R_{sy})^{-1} \) in CG

CG
> little current attenuation at output (if replace \( V_{sy} \) with \( V_{th} \in \text{equiv current source} \))

> MOSFET reproduces same current at output with high \( R \)
Common Drain amplifier (source follower)

(Fig 5.40, 6th edtion)

$\begin{align*}
\text{Small signal model (w/ } R_0) \\
\text{Rs}_{\text{sig}} &\quad \text{R}_{\text{L}} \\
\text{R}_{\text{in}} &\quad \text{R}_{\text{g}} \\
\text{V}_{\text{sig}} &\quad \text{V}_0
\end{align*}$

$\begin{align*}
\text{R}_{\text{in}} &= \frac{V_i}{i_i} = R_{\text{g}} \quad \text{since } i_g = 0 \\
V_i &= V_{\text{sig}} \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} = V_{\text{sig}} \frac{R_{\text{g}}}{R_{\text{g}} + R_{\text{sig}}} \\
R_0 &= \frac{V_i}{i_x} \quad \text{if } V_i = 0 \Rightarrow V_{\text{gs}} = 0 \Rightarrow i = 0
\end{align*}$
\[ R_0 = R_L \frac{1}{R_0 + 1/gm} \]

\[ V_0 = V_i \left[ \frac{R_L R_0}{R_L R_0 + 1/gm} \right] \Rightarrow AV = \frac{R_L R_0}{R_L R_0 + 1/gm} \]

\[ AV_0 = AV \mathbf{R_L = w} \approx \frac{R_0}{R_0 + 1/gm} \approx 1 \quad \text{(typically)} \]

Voltage at source follower follows that of gate \( \Rightarrow \) source follower

In many cases

\[ R_0 \gg R_L \Rightarrow AV \approx \frac{R_L}{R_L + 1/gm} \]

\[ G_V = \left( \frac{R_g}{R_g + R_{sy}} \right) \left( \frac{R_L R_0}{R_L R_0 + 1/gm} \right) \]

\[ G_V \approx 1 \quad \text{when} \quad R_g \gg R_{sy}, \ R_0 \gg 1/gm, \ R_L \quad \text{source follower} \quad \text{high } R_{in} \quad \text{low } R_{out}, \ AV \approx 1 \]

\[ \text{source follower} \quad \text{high } R_{in} \quad \text{low } R_{out}, \ AV \approx 1 \]

\[ \text{use as buffer in case where signal source has high internal resistance and load is low impedance} \]

\[ \Rightarrow \text{buffer amplifier} \]

\[ \Rightarrow \text{also used as last stage of multi-stage amplifier} \Rightarrow \text{provide high load current with loss of gain} \]
### Summary of amplifiers

<table>
<thead>
<tr>
<th>Type</th>
<th>Rin</th>
<th>Rout</th>
<th>Av0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS</td>
<td>∞</td>
<td>Rd</td>
<td>-g_m Rd</td>
</tr>
<tr>
<td>CS w/IRs</td>
<td>∞</td>
<td>Rd</td>
<td>-g_m Rd / (1 + g_m Rs)</td>
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<tr>
<td>CG</td>
<td>1/g_m</td>
<td>Rd</td>
<td>g_m Rd</td>
</tr>
<tr>
<td>source follower</td>
<td>∞</td>
<td>1/g_m</td>
<td>1</td>
</tr>
</tbody>
</table>

#### Current mirrors

Current mirrors are used for implementation of constant current source.

**Example**

![Current mirror circuit diagram](image)
Q1 & Q2 have same \( kn' \) & \( V_{tn} \)

\[
I_{D1} = \frac{1}{2} kn' (\frac{W}{L}) (U_{GS} - V_{tn})^2
\]

Q1 saturated

\[
I_{D1} = \frac{V_{DD} + V_{SS} - V_{GS}}{R}
\]

since gate current \( I_{G} \) = 0

Assume saturation for Q2

\[
I_{D2} = \frac{1}{2} kn' (\frac{W}{L}) (U_{GS} - V_{tn})^2
\]

\[
\Rightarrow I_{D2} = \frac{(W/L)^2}{(W/L)} I_{D1}
\]

\[\text{Fig. 8.2}\]

\[
\frac{I_{0}}{I_{ref}} = \frac{(W/L)^2}{(W/L)} \quad \text{for} \quad kn'_2 = kn'_1
\]

\[\text{Vo > Vov to ensure current mirror operation}\]
Fig 8.3  effect at finite $R_0$

- $Q_2$ operate at constant $V_Gs$ (fixed by $Q_1$)
- as $V_o$ changes, $I_o$ changes
- Finite output resistance

\[
R_0 = \frac{\Delta V_o}{\Delta I_o} = R_{o2} = \frac{V_{AQ2}}{I_o}
\]

8.2.2  Current steering: replication circuit in other locations

Fig 8.4
Q1, Q2, Q3 form 2 output current mirror

\[ I_2 = I_{ref} \left( \frac{W/L}{W/L_1} \right)^2 \]
\[ I_3 = I_{ref} \left( \frac{W/L}{W/L_1} \right)^3 \]

Need to ensure Q2 & Q3 in saturation

\[ V_{D2}, V_{D3} \geq -V_{SS} + V_{GS1} - V_T \]

\[ I_3 \] fed into PMOS current mirror Q4 & Q5

\[ I_5 = I_4 \left( \frac{W/L_5}{W/L_4} \right) \Rightarrow V_{DS5} \leq V_{DD} - |V_{DS1}| \]

for Q5 to remain in saturation

Q2 pulls current from circuit
Q5 pushes current from circuit

Q2 = current sink
Q5 = current source

Fig 8.5 Applications of Constant Currents

I2 & I5 generated in current steering circuit
Source follower
(Q 6)

Q2 is bias source

(a) Current source

Q5 pushes current into circuit

\[ V_{DD} \]
\[ I \]
\[ V_{csmin} \]

\[ V_0 < V_{DD} - V_{cs1min} \]

Active loaded ⇒ circuits that are current source loaded

(b) Current sink

Common source (Q 7)

\[ V_0 ≥ -V_{ss} \]

\[ V_{csmin} \]

\[ -V_{ss} \]