\[ I = A q_n \left( \frac{D_p}{L_p} n_{ph} + \frac{D_n}{L_n} n_{p0} \right) \left( e^{V_{th}} - 1 \right) \]

\[ n_{ph} = \frac{n_i^2}{N_D} \quad n_{p0} = \frac{n_i^2}{N_A} \]

\[ I = I_s \left[ e^{V_{th}} - 1 \right] \]

See 2 sides on current

\[ \text{Ex1: PN Junction} \]

\[ N_A = 10^{18} / \text{cm}^3 \quad N_D = 10^{16} / \text{cm}^3 \]

\[ A = 10^{-4} \text{ cm}^2 \]

\[ n_i = 1.5 \times 10^{10} / \text{cm}^3 \quad L_p = 5 \text{ um} \]

\[ L_n = 10 \text{ um} \]

\[ D_p = 10 \text{ cm}^2 / \text{s} \quad D_n = 18 \text{ cm}^2 / \text{s} \]

\[ I(V_{th}) = 0.1 \text{mA} \]

Find \( V_{th}, I_s, I_p/I_n \)

\[ I_s = \left[ \frac{10 \text{ cm}^2 / \text{s}}{(5 \times 10^{-4} \text{ cm})(1 \times 10^{10} / \text{cm}^3)} + \frac{18 \text{ cm}^2 / \text{s}}{(1 \times 10^{-4} \text{ cm}) (1 \times 10^{18} / \text{cm}^3)} \right] \]
\[ I_s = 7.3 \times 10^{-15} \text{ A} \]

\[ I = I_s (e^{V/V_T} - 1) \approx I_S e^{V/V_T} \text{ under forward bias} \]

\[ V = V_T \ln \left( \frac{I}{I_s} \right) = 0.025 eV \ln \left[ \frac{0.1 \times 10^{-3} \text{ A}}{7.3 \times 10^{-15} \text{ A}} \right] \]

\[ V = 0.584 \text{ V} \]

\[ I_P = A q \frac{D_P}{L_P} \frac{n_i^2}{N_D} (e^{V/V_T} - 1) \]

\[ I_N = A q \frac{D_N}{L_N} \frac{n_i^2}{N_A} (e^{V/V_T} - 1) \]

\[ \frac{I_P}{I_N} = \frac{J_P}{J_N} = 111 \Rightarrow \text{ hole current much greater than e current} \]

Makes sense since \( N_A/N_D \gg 100 \)

Reverse bias

- See slide

Current due to drift, very little diffusion

Breakdown - large reverse bias current

\( v \)

\( i \)
Zener breakdown highly doped pn junctions \[ \text{see slide} \]
\[ \text{IV}_1 > \text{IV}_2 \]

- E field in depletion region breaks covalent bonds & generates e/p pairs that are swept across junction by field
- Value limited by external circuit
- Usually for values \[ \text{IV}_2 \approx 5 \text{ V} \] or less

- Reverse voltage appearing between terminals, close to breakdown threshold \[ (\text{IV}_2) \]

Avalanche breakdown \[ \text{IV}_1 < \text{IV}_2 \]
\[ \text{see slide} \]

- Minority carriers that cross depletion region gain enough energy from electric field to knock electrons out of valence bond limit impact ionization

\[ e, p \rightarrow e & p \rightarrow 2(e & p) \text{ etc} \]

\[ \text{accelerate e/p} \]

Neither avalanche nor zener are destructive but heating from large currents & voltages in region can destroy diodes \[ \text{From Ch 4 eee.colorado.edu/mbart/book} \]
5.1.1 Most widely used transistor in integrated circuits

Fig 5.1 : NMOS transistors

- Source
- Gate
- Drain
- P substrate

= metal
| Oxide

- Body (B)

> Source Body (SB) & Drain Body (DB) are pn junctions kept reverse biased at all times

> Apply positive voltage to gate
> Current flows from Drain to Source

5.1.2 Operation with no gate voltage

> Between Drain & Source & back to back pn junctions (DB & BS)

> No current flow w/ Uos

> R ≈ 10^{12} Ω
5.1.3 Creating current

Fig 5.2

- When \( V_{GS} > 0 \), thin layer of electrons near surface form channel and create current path between drain & source.
- \( V_{GS} > 0 \) induces n-type layer
  \[ n^+(S) \rightarrow n \text{ (channel)} \rightarrow n^+(D) \]
- Called n-channel MOSFET or NMOS.
- \( V_{GS} = V_t \) is value that begins to induce inversion.
  \( V_t \approx V_T \) (thermal voltage).
- Typical \( 0.5 \, V < V_t < 1 \, V \)

Aside
- Gate and Channel form capacitor.
  - Oxide = capacitor dielectric.
- \( V_{GS} > 0 \) means positive charge on
top of gate electrode and negative charge in induction channel

> Results in electric field that controls amount of charge in channel and conductivity \( \Rightarrow \text{Field effect transistor} \)

5.1.4 Applying small \( V_{BS} \), \( V_{DS} \sim 50\text{mV} \)

\[ \frac{I_s}{I} = \frac{V_{GS}}{I} \]

\[ V_{DS} \sim 50\text{mV} \]

Induced n channel

P type substrate

> \( V_{DS} \) causes current \( I_D \) to flow through n channel

> Electrons flow \( S \rightarrow D \), current flows \( D \rightarrow S \)

> When \( V_{GS} = V_t \), electron concentration negligible (no current)

> As \( V_{GS} \) increases, electron concentration, conductance \( (\sim \text{resistance}) \), channel conductance \( \propto (V_{GS} - V_t) \)

> \( I_D \propto V_{DS} \) (and \( V_G = 0 \))
Fig 5.4

\[ i_D \text{ vs } U_{DS} \text{ (Nmos transisistor)} \]

*For small \( U_{DS} \)

\[ U_{DS} \]

\[ V_{GS-B} \]

\[ V_{GS-A} \]

\[ k_n = \mu_n C ox W/L \]

Slope: \( G_{DS} = k_n V_{ov} \)

\[ V_{ov} = V_{GS} - V_t = \text{overdrive voltage} \]

Graph describes enhancement mode MOSFET Nmos that conducts when channel is induced (contrast with depletion mode MOSFET with opposite behavior).

Section 5.15 Operation as \( U_{DS} \) Increases

> Hold \( V_{GS} \) constant at value \( > V_t \)

> \( U_{DS} \) is voltage drop across length of channel \( \Rightarrow \) non uniform voltage across channel
Fig 5.5  Enhancement N MOS

> Finite voltage drop across channel
  \[ V_{DS} \]
> Channel depth depends on voltage difference between gate & channel
> Channel depth decreases as approach drain

> Variation in channel depth
  I/V curve bends over \( \Rightarrow \) triode region

Fig 5.6  Triode mode of operation

Solid line = voltage drop across channel

\[ V_{DS} \]

Channel shape \( \leq (V_{OV} - V_{DS}) \)
> When $V_{DS} = V_{GS} - V_{T}$

channel depth = 0 at drain

> Further increase in $V_{DS}$ does not change

channel shape $\rightarrow$ no change in $I_D$ $\rightarrow$

saturation

$V_{DSat} = V_{GS} - V_{T}$

**Figure 5.7**

Triode $\rightarrow$ saturation

$V_{DS} < V_{OV}$ $\rightarrow$ $V_{DS} > V_{OV}$

almost linear

**Figure 5.8** saturation mode

Triode bends channel resistance in $V_{DS}$

Saturation current saturates because channel pinched off at drain

Channel shape

Channel pinches off
Section 5.1.6 $i_D \text{ vs } V_{dc}$ relationship

Reference: ecee.colorado.edu/~bart/book/ch7

Capacitance
\[
C_{ox} = \frac{\varepsilon_{ox}}{\varepsilon_{o}}
\]

$\varepsilon_{ox} = 3.9 \varepsilon_0$ for SiO$\text{2}$

A strip of $w \cdot dx \Rightarrow dC = C_{ox} \cdot w \cdot dx$

Charge under strip? $dq = -C_{ox} (w \cdot dx) \cdot [V_{gs} - V(x) - V_t]$

> Charge proportional to channel shape shown on previous page

> Minus sign due to electrons, i.e., $N_D$.

> Device voltage produces electric field

\[
E_x = -\frac{dV(x)}{dx}
\]

$E$ field causes drift of electrons

$V_{drift} = \frac{dx}{dt} = -\mu_n \cdot E_x \cdot (x) = \mu_n \frac{dV(x)}{dx}$

Drift current

\[
i = \frac{\partial q}{\partial t} = \frac{\partial q}{\partial x} \cdot \frac{dx}{dt}
\]

\[
i = -\mu_n \cdot C_{ox} \cdot w \cdot [V_{gs} - V(x) - V_t] \cdot \frac{dV(x)}{dx}
\]

Notes:
1. $i_D$ is independent of $x$
2. $i_D = -i$ (definition of $i_D$)
Substitute $i_D = -i$ and integrate over channel length

$$\int_0^L i_D \, dx = \int_0^{V_{DS}} \mu_n C_{ox} W \left[ V_{GS} - V(X) - V_T \right] \, dV$$

$$i_D = \mu_n C_{ox} \frac{W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$i_D$ reaches maximum value when $V_{DS} = V_{GS} - V_T$ (beginning of saturation)

**Summary**

$$i_D = \begin{cases} 
\frac{kn'}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] & \text{triode} \quad V_{DS} < V_{OV}, \quad V_{GS} > V_T \\
\frac{kn'}{L} \left[ V_{GS} - V_T \right]^2 & \text{saturation} \quad V_{DS} \geq V_{OV}, \quad V_{GS} > V_T 
\end{cases}$$

$k_n' = \mu_n C_{ox}$ \quad trans conductance parameter \quad $[A/V^2]$

$$i_D \propto \frac{W}{L} \quad \text{as aspect ratio}, \quad W \text{ limited by available size}$$

$L_{\text{min}}$ = minimum channel size set by process parameters
Ex 5.1

Consider process technology for which
$L_{min} = 0.4 \text{ µm}, \quad t_{ox} = 8 \text{ nm}, \quad \mu n = 450 \text{ cm}^2/\text{V-s}, \quad V_t = 0.7 \text{ V}, \quad \varepsilon_{ox} = 3.45 \times 10^{-11} \text{ F/m}

a) Find $C_{ox}$ & $k_n'$

b) For MOSFET w/ $W/L = 8\text{ µm}/0.8\text{ µm}$
calculate $V_{ov}$, $V_{gs}$, $V_{ds,min}$ to operate in saturation region w/ $I_{DS} = 100 \text{ mA}$

c) For device in (b), find $V_{ov}$ & $V_{gs}$
to cause device to operate as 1kΩ resistor for small $V_{ds}$

Solution

a) $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.45 \times 10^{-11} \text{ F/m}}{8 \times 10^{-9} \text{ m}}$

\[ C_{ox} = 4.32 \times 10^{-3} \text{ F/m}^2 \]

\[ k_n' = \mu n C_{ox} = (450 \text{ cm}^2/\text{V-s})(4.32 \times 10^{-3} \text{ F/m}^2)(10^{-4} \text{ m}^2/\text{cm}^2) \]

\[ k_n' = 1.94 \times 10^{-4} \text{ A/V}^2 \]

b) To operate in saturation

\[ I_D = \frac{1}{2} k_n' \frac{W}{L} V_{ov}^2 \]

100 mA = $\frac{1}{2} (1.94 \text{ mA/V}^2)(8/0.8)V_{ov}^2$

$V_{ov} = 0.32 \text{ V}$
\[ V_{GS} = V_{OV} + V_t = 1.02\, V \]
\[ V_{DS\, min} = V_{OV} = 0.32\, V \]

(42)

(c) For MOSFET in triode region &

\[ V_{DS}\, small \]

\[ R_{DS} = \frac{1}{k_n' \frac{W}{L} \, V_{OV}} \]

\[ 1000\, \Omega = \frac{1}{(1.94 \times 10^{-6} \frac{A}{V^2}) \left( \frac{8}{0.8} \right) V_{OV}} \]

\[ V_{OV} = 0.52\, V \]

\[ V_{OV} = V_{GS} - V_t \]

\[ V_{GS} = 1.22\, V \]