What does FinFet look Like

Bulk nmos

Silicon on insulator

FinFet

From Haiying Zhao
What does FinFet look like

Fig. 1. Schematic of a FinFET structure.

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From FD/SOI to FinFET

Bend up the gate and narrow the gate. Fin width = 2* film thickness
The effect body thickness is reduced by 2. Xd can be regarded as Fin width /2. To obtain good control of SCE, Leff > 1.5*Wfin (Fin width).
Finfet can operate at two mode, single gate and double gate.
FinFet characteristics

Lg = 15nm

Some values:
Threshold Voltage = 0.196 V
Subthreshold Slope = 72 mV/decade
Off Current = 70 ηA/μm
DIBL = 64.67 mV/V

From Haiying Zhao
Approximate dc I-V equations?

Square law?
One way is using nth power law to compute the FinFet current.

\[
I_D = \frac{W_{\text{eff}}}{L_{\text{eff}}} B (V_{\text{GS}} - V_{\text{th}})^n
\]

where

\[
\begin{align*}
V_{\text{DSat}} &= K(V_{\text{GS}} - V_{\text{th}})^m \\
V_{\text{DS}} &\geq V_{\text{DSat}} : \text{saturated region}
\end{align*}
\] (2)

\[
I_D = I_{\text{DSat}} \left( 2 - \frac{V_{\text{DS}}}{V_{\text{DSat}}} \right) \frac{V_{\text{DS}}}{V_{\text{DSAT}}}
\]

when \( V_{\text{DS}} < V_{\text{DSat}} \) : linear region \hspace{1cm} (3)

\[
I_D = 0, \quad \text{when} \ V_{\text{GS}} < V_{\text{th}} : \text{cutoff region}
\] \hspace{1cm} (4)

From Haiying Zhao
FinFet: Challenges or Opportunities

Carrier mobility:
   Lightly doped or undoped fin body increases carrier mobility.
   Short channel length enables velocity overshoot, which increases mobility.
   Low Vth decreases the vertical electric field, which increases carrier mobility.

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