

CONTROL METHOD FOR LOW-VOLTAGE DC POWER SUPPLY IN BATTERY- POWERED SYSTEMS WITH POWER MANAGEMENT

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Abstract - The paper describes a control method for operating a variable switching frequency buck converter, designed to convert an input battery voltage of 4.5 to 8Vdc to an output voltage of 3.3Vdc with a maximum load current of 4Adc. The advantages of the control method are that the output voltage is tightly regulated and that high efficiency (over 90%) is maintained over a very wide range of load currents (40mA to 4Adc). The output voltage ripple, DC and transient voltage regulation (for 100:1 load transients) are within $\pm 1\%$ of the nominal output voltage. These advantages are particularly important for battery-powered systems with power management.

1 Introduction

In recent years, much attention has been given to various aspects of low-power electronics design because of numerous and widespread applications in wireless communication systems, portable computers, implantable medical devices etc. For a given battery charge, the system operating life, which is one of important performance criteria, is directly affected by efficiency of power converters used to distribute regulated supply voltages. As a result, power converter design has become an important component in the design of low-power electronics [1].

Unique aspects of the power-converter design for battery-powered and other systems with power management include the requirements to maintain a tightly regulated, low-ripple output dc voltage (3.3V or less) for a very wide range of loads, and subject to zero-load to full-load transients. Similar requirements are imposed by the new generation of high-speed microprocessors [2].

For the task of regulating a low dc voltage from an unregulated dc source (battery), we consider the standard buck converter configuration with a synchronous rectifier used to

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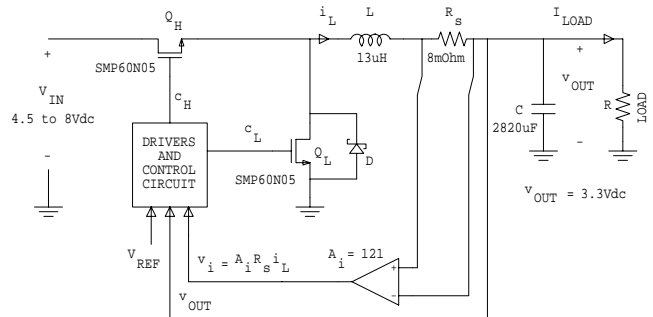


Figure 1: Schematic of the 13W power stage.

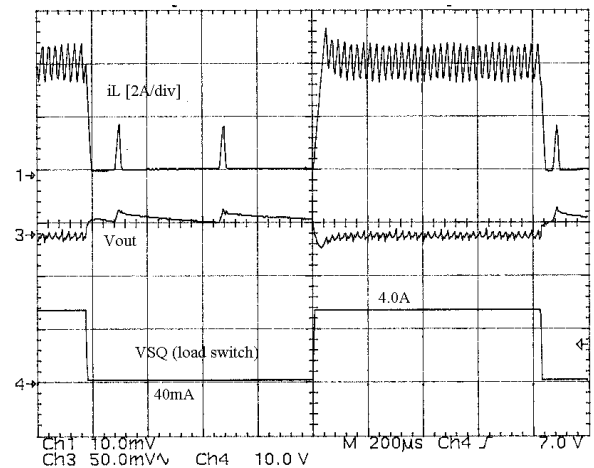


Figure 2: 40mA-to-4A load transient response in the experimental converter of Fig. 1 at $V_{IN} = 5V$. Top to bottom: inductor current i_L , output voltage v_{OUT} , load switch control V_{SQ} .

improve efficiency [1]-[3]. Our experimental power converter is shown in Fig. 1. To maintain high efficiency at very light loads, switching losses must be reduced by reducing the switching frequency, and the converter is operated in the discontinuous conduction mode (DCM). An analysis of power losses and the

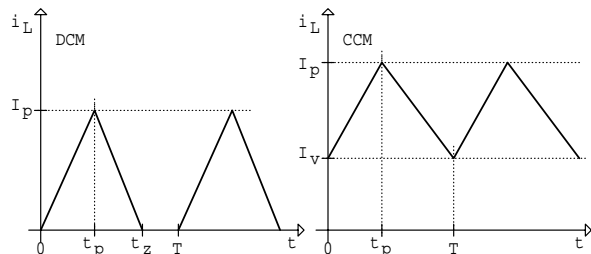


Figure 3: Inductor current waveform in the discontinuous-conduction mode (left) and the continuous-conduction mode (right).

selection of the peak inductor current to optimize efficiency in DCM have been described in [4]. As the load increases, the converter moves into the continuous conduction mode (CCM) and the inductor current ripple (or the switching frequency) can be used as a parameter to optimize efficiency. The purpose of this paper is to describe a control method to accomplish operation in different operating modes for the purpose of maintaining high efficiency in a very wide range of loads and fast large-signal transient response, as illustrated by the experimental waveforms of Fig. 2.

The power stage used in experimental verification is described in Section 2. Section 3 described the proposed control method and its implementation. Analyses of the converter/controller operation, the output voltage ripple, as well as DC and transient voltage regulation are presented in Section 4. Results of experimental verification are in Section 5 of the paper.

2 Power Stage

Fig. 1 shows a schematic of the experimental 13W buck converter with synchronous rectifier. The power stage converts a battery voltage, V_{IN} , to the desired regulated output voltage, v_{OUT} . V_{IN} ranges from 4.5 to 8Vdc, while v_{OUT} is regulated at 3.3Vdc. The DC load current is in the range $0 < I_{LOAD} < 4A$. The high side switch, Q_H , is controlled by control signal c_H . The low side switch, Q_L , which is the synchronous rectifier, is controlled by control signal c_L . The inductor current, i_L , is sensed by resistor R_s and a differential amplifier to produce control signal v_i . The gain of the differential amplifier is chosen so that v_i is about 1 volt when i_L is 1 amp. The desired output voltage is set by V_{REF} which is 3.3Vdc in this case.

3 Control Method

The converter operates in the discontinuous conduction mode at light loads and in the continuous conduction mode at higher loads. Typical inductor current waveforms in the two modes are shown in Fig. 3.

In the DCM, the output voltage regulation is based on sensing the output voltage ripple on v_{OUT} , so that the ripple stays approximately the same, and the transient response has no overshoots or undershoots. The peak inductor current I_p is preset at a constant value so that the efficiency in DCM is at maximum, as described in [4]. The controller operates as follows: initially both switches are off. When capacitor C is

discharged by the load to the DC reference voltage V_{REF} , Q_H is turned on. The inductor current i_L ramps up to I_p and then Q_H is turned off. While i_L ramps down to zero, Q_L is turned on. Switch Q_L provides the synchronous rectification and is turned off when i_L reaches zero amps. The current in the inductor causes a pulse of charge which increases v_{OUT} by charging C. Capacitor C is discharged by the load, thus repeating the process. The converter operates in the DCM if $I_{LOAD} \leq (1/2)I_p$.

In the CCM, the output voltage can no longer be regulated based on the output voltage ripple only. The sensed inductor current is used to accomplish a hysteretic current-mode control: Q_H is turned on when the inductor current reaches a minimum, called the valley inductor current, I_v , and off when the maximum inductor current, called the peak inductor current, I_p , is reached. The values of I_v and I_p are determined by the control circuit, as discussed in the following section on implementation.

3.1 Controller Implementation

Fig. 4 shows a block diagram of the control circuit. The output voltage v_{OUT} is followed by an optional switching noise filter and then goes to an amplifier. The difference between the desired output voltage V_{REF} and the actual output voltage is multiplied by the voltage-loop error amplifier with gain A_v . The result passes through a limiter, LIM_v , and the resulting signal is control signal v_v . A constant value V_{Ripple} , is added to v_v . The result passes through a limiter, LIM_p , and the resulting signal is control signal v_p . The v_p signal cannot go below V_{pDCM} , thus providing a minimum peak current in the DCM. The v_v signal cannot go above V_{vmax} , therefore the v_p signal cannot go above $V_{vmax} + V_{Ripple}$, thus providing a current limit protection.

The i_L signal develops a voltage across resistor R_s and this is amplified by A_i to get the v_i signal. The comp1 output is high when $v_i < v_v$, and will set the latch L_H and reset the latch L_L . The c_L signal will go low in the CCM or stay low in the DCM, causing the low side switch to go low or stay low. The c_H signal will go high after a delay t_{dH} , causing the high side switch to turn on and the inductor current i_L to ramp up. This can occur in both the CCM and the DCM. In the DCM the signal v_i will be zero, ideally, when the comp1 output goes high. Note that when $v_v = 0$, $v_{OUT} = V_{REF}$.

The comp2 output is high when $v_i > v_p$, and will set L_L and reset L_H . The c_H signal will go low, causing the high side switch to turn off and i_L to ramp down. The c_L signal will go high after a delay t_{dL} , providing synchronous rectification. This can occur in both the CCM and the DCM.

The comp3 output is high when $v_i < V_{offset}$ and will reset L_L . The signal c_L will go low and the low side switch will turn off. This occurs in the DCM and is necessary to prevent i_L from changing direction after it ramps down to zero amps. The DC signal V_{offset} is used to ensure that the synchronous rectifier is turned off before i_L changes polarity through the synchronous rectifier Q_L .

Delays t_{dH} and t_{dL} are used to prevent both the high and low switches from being on at the same time, a condition known as shoot-through.

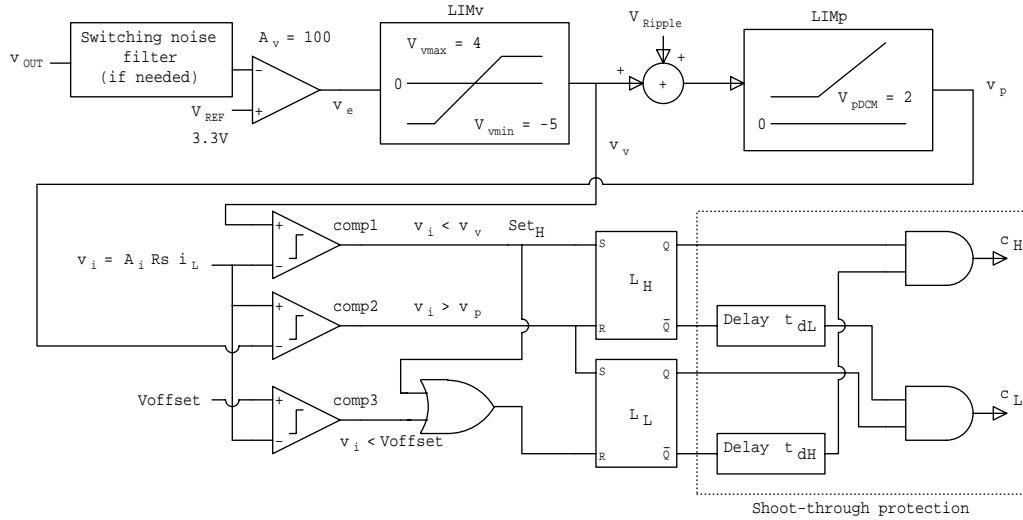


Figure 4: Block diagram of the control circuit.

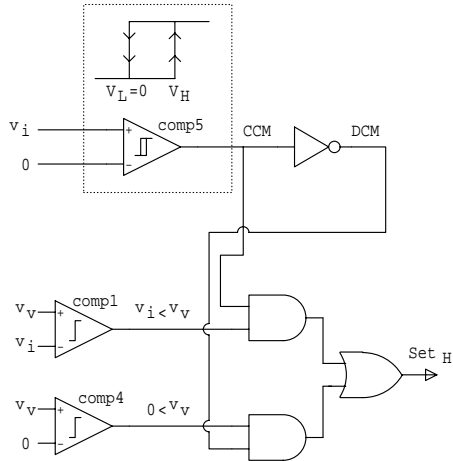
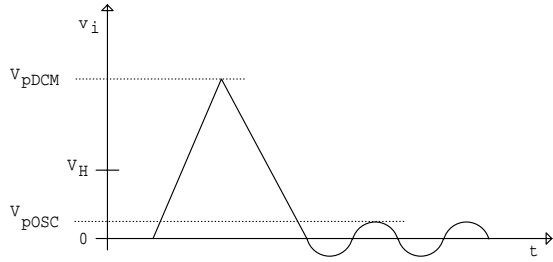


Figure 5: Modification of the controller circuit because of DCM ringing due to parasitics.

Because there is some parasitic capacitance at the switching node, the inductor will exchange current with the parasitic capacitance, and the inductor current will have a small oscillation around zero amps for some time after the inductor current crosses zero. The control circuit may be modified to take this into account. The modification replaces the comp1 output which produces the signal Set_H with the circuit shown in Fig. 5. The peak amplitude of the v_i signal due to the oscillation occurring after the inductor current crosses zero is called V_{pOSC} . The comparator comp5 is implemented with hysteresis

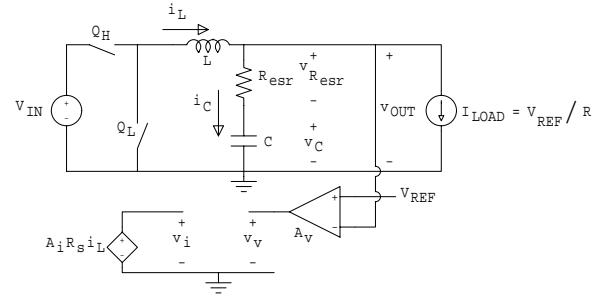


Figure 6: Simplified power stage circuit for analysis of operation.

voltages V_L and V_H where $V_L = 0$ and $V_{pOSC} < V_H < V_{pDCM}$. The comp5 output goes low when $v_i < V_L$ and goes high when $v_i > V_H$. If the comp5 comparator output is high it indicates the CCM and if the output is low it indicates the DCM. The CCM signal is used to gate comp1 so that $v_i < v_v$ sets the high switch, as before. The DCM signal is used to gate comp4 which goes high if $0 < v_v$, and then this signal sets the high switch. Thus v_v is compared to 0 in the DCM.

4 Analysis of Operation

The purpose of this section is to analytically describe various controller/converter operating modes and to derive results needed for the design: expressions for the output voltage ripple, DC and transient voltage regulation.

Fig. 6 shows the simplified circuit used in the analysis. The analysis assumes the output voltage ripple is small and can be neglected in the calculation of the inductor current waveform and load current. Also, the MOSFET resistance, inductor series resistance, and the current sense resistance are considered negligible so that the inductor current waveform increases or decreases with a constant slope for given input and output voltages. The capacitor equivalent series resistance, R_{esr} , is included in the model.

From Fig. 6 we get the control signals v_i and v_v :

$$v_i = A_i R_s i_L, \quad (1)$$

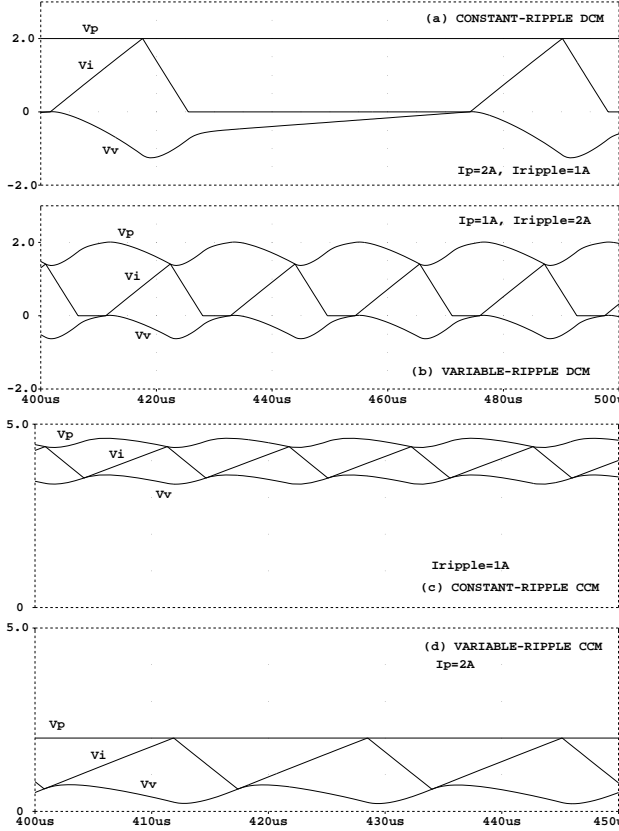


Figure 7: Controller waveforms v_v , v_i and v_p in various operating modes as obtained by simulation using the component values given in the power stage of Fig. 1. The bandwidth of the voltage amplifier is 100kHz, and the capacitor equivalent series resistance is $R_{\text{esr}} = 5m\Omega$. Top to bottom: waveforms in the DCMcr, DCMvr, CCMcr and CCMvr modes.

$$v_v = A_v (V_{\text{REF}} - v_{\text{OUT}}). \quad (2)$$

The load current is $I_{\text{LOAD}} = \frac{V_{\text{REF}}}{R}$, and the capacitor current is $i_C = i_L - I_{\text{LOAD}}$. The output voltage waveform is then given by

$$v_{\text{OUT}}(t) = (i_C)R_{\text{esr}} + v_C(0) + \int_0^t (i_C)d\tau. \quad (3)$$

Because $v_i = v_v$ when the high switch turns on and $v_i = v_p$ when the high switch turns off and the low switch turns on, Eq. (1) gives the following for the inductor valley current,

$$I_v = \frac{v_v(0)}{A_i R_s}, \quad (4)$$

the inductor peak current,

$$I_p = \frac{v_p(t_p)}{A_i R_s}, \quad (5)$$

and the inductor current ripple is defined by $I_{\text{ripple}} = I_p - I_v$.

4.1 Discontinuous Conduction Mode

The inductor current in the DCM, as shown in Fig. 3, is given by:

$$i_L(t) = \begin{cases} \frac{I_p}{t_p}t, & 0 \leq t \leq t_p \\ I_p - \frac{I_p}{t_z - t_p}(t - t_p), & t_p \leq t \leq t_z \\ 0, & t_z \leq t \leq T \end{cases} \quad (6)$$

The times t_p and t_z are:

$$t_p = \frac{I_p L}{V_{\text{IN}} - V_{\text{REF}}}, \quad t_z = t_p + \frac{I_p L}{V_{\text{REF}}}. \quad (7)$$

The values for $v_{\text{OUT}}(0)$, I_p , and I_v will depend on the mode that the converter operates in. There are two DCM modes: the DCM constant ripple mode, DCMcr, with the typical controller waveforms shown in Fig. 7(a), and the DCM variable ripple mode, DCMvr, with the typical waveforms shown in Fig. 7(b).

In both DCM modes,

$$I_v = 0. \quad (8)$$

From Eqs. (2), (4), and (8), it follows that

$$v_{\text{OUT}}(0) = V_{\text{REF}}. \quad (9)$$

From Eqs. (3), (6), and (9), we find $v_{\text{OUT}}(t)$ in the three subintervals:

$$v_{\text{OUT}}(t) = V_{\text{REF}} + \left(\frac{I_p}{t_p}t\right)R_{\text{esr}} + \frac{I_p t^2}{2C t_p} - \frac{I_{\text{LOAD}}}{C}t, \quad 0 \leq t \leq t_p, \quad (10)$$

$$\begin{aligned} v_{\text{OUT}}(t) &= V_{\text{REF}} + \frac{I_p t_p}{2C} - \frac{I_{\text{LOAD}} t_p}{C} + \\ &+ \left(I_p - \frac{I_p}{(t_z - t_p)}(t - t_p)\right)R_{\text{esr}} + \\ &- \frac{I_p}{2C(t_z - t_p)}(t - t_p)^2 + \frac{(I_p - I_{\text{LOAD}})}{C}(t - t_p), \quad t_p \leq t \leq t_z, \end{aligned} \quad (11)$$

and

$$v_{\text{OUT}}(t) = V_{\text{REF}} + \frac{I_p t_z}{2C} - \frac{I_{\text{LOAD}}}{C}t, \quad t_z \leq t \leq T \quad (12)$$

Because $v_{\text{OUT}}(0) = v_{\text{OUT}}(T)$,

$$\frac{I_{\text{LOAD}} T}{C} = \frac{I_p t_z}{2C}, \quad (13)$$

and using Eq. (7), we find that the switching frequency in the DCM is proportional to the load current:

$$f_s = 1/T = I_{\text{LOAD}} \frac{2V_{\text{REF}}(V_{\text{IN}} - V_{\text{REF}})}{I_p^2 L V_{\text{IN}}}. \quad (14)$$

The DCMcr mode occurs in the DCM when $V_{\text{pDCM}} \geq v_v(t_p) + V_{\text{ripple}}$. In this case, $v_p(t_p) = V_{\text{pDCM}}$ and from Eq. (5) we have

$$I_p = \frac{V_{\text{pDCM}}}{A_i R_s}. \quad (15)$$

The DCMvr mode occurs in the DCM when $V_{p\text{DCM}} < v_v(t_p) + V_{\text{Ripple}}$. In this case, $v_p(t_p) = v_v(t_p) + V_{\text{Ripple}}$ and from Eq. (5) it follows that

$$I_p = \frac{(v_v(t_p) + V_{\text{Ripple}})}{A_i R_s}. \quad (16)$$

Because the output voltage ripple changes with load current in the DCM, the peak inductor current changes with load current in the DCMvr mode. All other parameters are the same as in the DCMcr mode.

Analysis of the output voltage waveforms allows calculation of the peak-to-peak output voltage ripple. In the DCMcr mode, the maximum ripple will occur at the lowest load current. Assuming that the load current is very close to zero, the minimum output voltage is V_{REF} because the controller turns on the high switch Q_H when $v_{\text{OUT}} = V_{\text{REF}}$. The maximum output voltage occurs on or after t_p depending on the $R_{\text{esr}}C$ time constant, where R_{esr} is the equivalent series resistance of the output filter capacitor C . For the peak-to-peak output voltage ripple in the DCM, we get:

$$\Delta v_{\text{OUT}} = \begin{cases} \frac{I_p t_z}{2C} \left(1 + \frac{(CR_{\text{esr}})^2}{t_z(t_z - t_p)}\right), & CR_{\text{esr}} \leq (t_z - t_p) \\ R_{\text{esr}} I_p \left(1 + \frac{t_p}{2CR_{\text{esr}}}\right), & CR_{\text{esr}} \geq t_z - t_p \end{cases} \quad (17)$$

4.2 Continuous Conduction Mode

In the CCM, the load current is given by

$$I_{\text{LOAD}} = \frac{I_p + I_v}{2}, \quad (18)$$

and the inductor current, as shown in Fig. 3, is:

$$i_L(t) = \begin{cases} I_v + \frac{I_{\text{ripple}}}{t_p} t, & 0 \leq t \leq t_p \\ I_p - \frac{I_{\text{ripple}}}{T - t_p} (t - t_p), & t_p \leq t \leq T \end{cases} \quad (19)$$

The high switch on time t_p and the switching period T are given by

$$t_p = \frac{I_{\text{ripple}} L}{V_{\text{IN}} - V_{\text{REF}}}, \quad T = t_p + \frac{I_{\text{ripple}} L}{V_{\text{REF}}} \quad (20)$$

From Eq. (2), we have

$$v_{\text{OUT}}(0) = V_{\text{REF}} - \frac{v_v(0)}{A_v}, \quad (21)$$

and the output voltage waveforms in the two subintervals are given by

$$v_{\text{OUT}}(t) = \frac{I_{\text{ripple}}}{t_p} R_{\text{esr}} t + V_{\text{REF}} - \frac{v_v(0)}{A_v} + \frac{I_{\text{ripple}}}{2C} \left(\frac{t}{t_p} - 1\right) t, \quad 0 \leq t \leq t_p, \quad (22)$$

and

$$v_{\text{OUT}}(t) = I_{\text{ripple}} \left(1 - \frac{t - t_p}{T - t_p}\right) R_{\text{esr}} + V_{\text{REF}} - \frac{v_v(0)}{A_v} + \frac{I_{\text{ripple}}}{2C} \left(1 - \frac{t - t_p}{T - t_p}\right) (t - t_p), \quad t_p \leq t \leq T, \quad (23)$$

Using the expressions for the output voltage waveform, the peak-to-peak output voltage ripple can be calculated for the CCM:

$$\Delta v_{\text{OUT}} = \begin{cases} \frac{I_{\text{ripple}} T}{8C} \left(1 + \frac{8(CR_{\text{esr}})^2}{T(T - t_p)}\right), & CR_{\text{esr}} \leq (T - t_p)/2 \\ R_{\text{esr}} I_{\text{ripple}} \left(1 + \frac{2t_p - T}{8CR_{\text{esr}}}\right), & CR_{\text{esr}} \geq (T - t_p)/2 \end{cases} \quad (24)$$

The worst case is at the DCM-CCM boundary where $I_p = 2I_{\text{LOAD}}$.

There are two CCM modes as illustrated by the waveforms of Fig. 7(c) and (d). In both CCM modes, from Eq. (18), we have

$$I_v = 2I_{\text{LOAD}} - I_p \quad (25)$$

and from Eqs. (4) and (25),

$$v_v(0) = 2I_{\text{LOAD}} A_i R_s - I_p A_i R_s. \quad (26)$$

The CCMvr (variable-ripple CCM) mode occurs in the CCM when $V_{p\text{DCM}} \geq v_v(t_p) + V_{\text{Ripple}}$. In this case, $v_p(t_p) = V_{p\text{DCM}}$ and from Eq. (5),

$$I_p = \frac{V_{p\text{DCM}}}{A_i R_s}. \quad (27)$$

The CCMcr (constant-ripple CCM) mode occurs in the CCM when $V_{p\text{DCM}} \leq v_v(t_p) + V_{\text{Ripple}}$. In this case, $v_p(t_p) = v_v(t_p) + V_{\text{Ripple}}$ and from Eq. (5),

$$I_p = \frac{v_v(t_p) + V_{\text{Ripple}}}{A_i R_s}. \quad (28)$$

Assuming the voltage-loop error amplifier and switch noise filter bandwidths do not significantly affect the $v_v(t)$ signal, $v_v(t_p)$ can be obtained from Eqs. (22) and (2):

$$v_v(t_p) = v_v(0) - I_{\text{ripple}} R_{\text{esr}} A_v. \quad (29)$$

Using Eqs. (21), (22), (23), and (26), and the above equations for I_p the output voltage waveform can be obtained.

4.3 DC Voltage Regulation Analysis

In the DCM, from Eq. (9), the DC value of v_{OUT} will be V_{REF} plus some additional voltage due to the voltage ripple on v_{OUT} .

In the CCM, the DC value of v_{OUT} depends on V_{REF} , I_{LOAD} , A_v , $A_i R_s$, and I_{ripple} .

In the CCMvr, Eqs. (21), (26), and (27) can be used to determine the DC value of v_{OUT} .

In the CCMcr, Eqs. (21), (26), and (28) can be used to determine the DC value of v_{OUT} . If the ripple on v_v is significantly smaller than the ripple on v_i , then Eq. (28) becomes

$$I_p \approx \frac{v_v(0) + V_{\text{Ripple}}}{A_i R_s} \quad (30)$$

This simplifies Eq. (26) to

$$v_v(0) = I_{\text{LOAD}} A_i R_s - \frac{V_{\text{Ripple}}}{2}, \quad (31)$$

which can then be used in place of Eq. (26) to determine v_{OUT} and the DC voltage regulation.

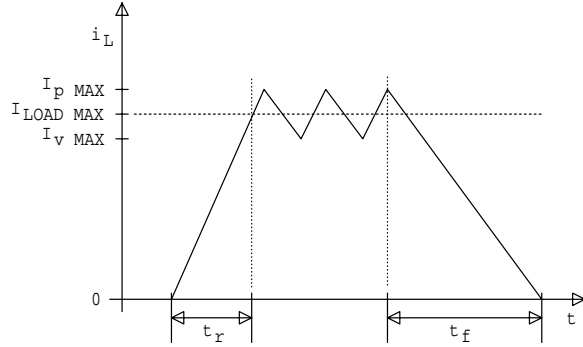


Figure 8: Inductor current waveform in the zero-load-to-full-load transient.

4.4 Transient Voltage Regulation Analysis

Fig. 8 shows the inductor current transient waveforms where the load current goes from 0 to $I_{LOAD\ MAX}$ and back to 0. The inductor current rise and fall times are:

$$t_r = \frac{LI_{LOAD\ MAX}}{V_{IN} - V_{REF}}, \quad t_f = \frac{LI_{p\ MAX}}{V_{REF}}. \quad (32)$$

The inductor current waveform can be used to find the change in the output voltage:

$$\Delta v_{OUT} = \begin{cases} -\frac{t_r I_{LOAD\ MAX}}{2C} \left(1 + \frac{(CR_{est})^2}{t_r^2}\right), & CR_{est} \leq t_r \\ -R_{est} I_{LOAD\ MAX}, & CR_{est} \geq t_r \end{cases} \quad (33)$$

for the zero-to-full-load transient, and

$$\Delta v_{OUT} = \begin{cases} \frac{t_f I_{p\ MAX}}{2C} \left(1 + \frac{(CR_{est})^2}{t_f^2}\right), & CR_{est} \leq t_f \\ R_{est} I_{p\ MAX}, & CR_{est} \geq t_f \end{cases} \quad (34)$$

for the full-to-zero-load transient.

5 Experimental Results

The controller allows for the setting of the peak inductor current in the discontinuous conduction mode using the parameter V_{pDCM} , and the inductor ripple current in the continuous conduction mode using the parameter V_{Ripple} . These two parameters are found so as to maximize the converter efficiency throughout the load range.

Fig. 9 is a plot of the converter efficiency versus the peak inductor current in the DCM with input voltages of 5Vdc and 8Vdc. Fig. 10 is a plot of the converter efficiency versus the inductor ripple current in the CCM at input voltages of 5Vdc and 8Vdc. From these plots it was determined that operating the converter with a DCM peak inductor current of 2A and an inductor ripple current of 2A would give good efficiency results over a wide range of loads without causing excessive output voltage ripple. Therefore the converter was adjusted to operate in the DCMcr and CCMcr modes by adjusting the V_{pDCM} and V_{Ripple} controls to give the 2A inductor peak and ripple current.

Fig. 11 is a plot of converter efficiency versus load current with input voltages of 5Vdc and 8Vdc. The efficiency is over

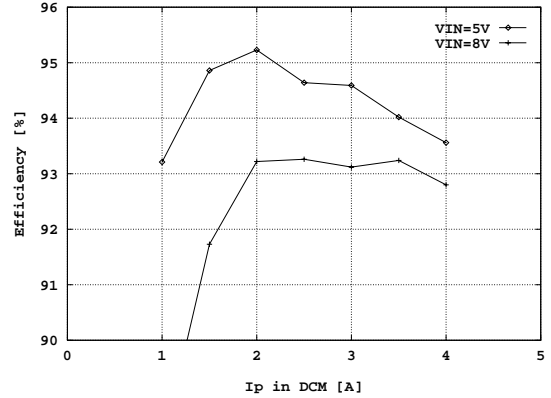


Figure 9: Efficiency of the experimental converter as a function of the peak inductor current I_p in the discontinuous conduction mode at $I_{LOAD} = 40\text{mA}$ load $V_{IN} = 5\text{V}$ and $V_{IN} = 8\text{V}$.

90% for both input voltages over the entire range of load currents, from 40mA to 4.0A.

The maximum load current was specified as 4Adc. With a 2A ripple current, the inductor valley current at full load is 3A and the peak current is inductor current is 5A. The current gain $A_i R_s$ was chosen to be approximately 1V/A, so $v_v(0) = 3V$ at the maximum load current. From Eq. (21) it is seen that a voltage-loop error amplifier with a gain of $A_v = 100$ gives a dc regulation of about 1%. Fig. 12 is a plot of the output voltage versus load current. The output voltage changes about 40mV, giving good agreement with theory. The maximum switching frequency in the experimental converter was $f_s = 70\text{kHz}$ for the maximum load current and $V_{IN} = 8\text{V}$.

Figs. 2, 13 and 14 show the transient response of the power converter in various modes of operation. A squarewave signal, V_{SQ} , is used to cause the load current to change from a maximum value, when the squarewave is high, to a minimum value, when the squarewave is low. The time varying waveforms i_L , ac-coupled v_{OUT} , and V_{SQ} are shown. All three sets of waveforms show that the output voltage stays within $\pm 1\%$ of the nominal value, which includes ripple, transient and DC voltage regulation.

6 Conclusions

A control method for low-voltage dc power supply based on the buck converter with synchronous rectifier is described in this paper. The controller is constructed so that the output voltage is well regulated and high efficiency is maintained for a very wide range of loads, including large-signal load transients from almost zero to full load. At light loads, the converter is operated in the variable-frequency, discontinuous conduction mode where the peak inductor current is set to the value that maximizes the efficiency. At higher loads, the converter is operated in the continuous conduction mode where the inductor current ripple is selected to maximize efficiency. To illustrate the controller and the power-stage design, an experimental converter is constructed to regulate the output dc voltage at 3.3V from an unregulated dc input in the 4.5V to 8V range,

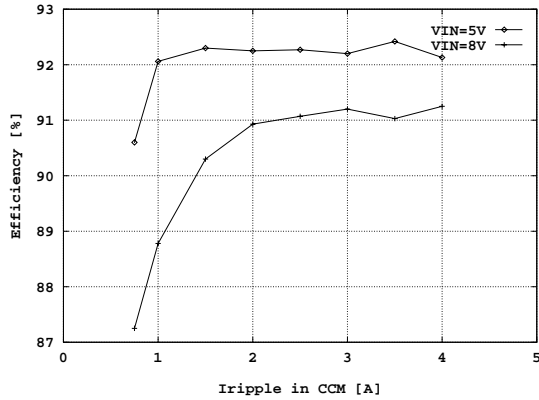


Figure 10: Efficiency of the experimental converter as a function of the inductor ripple current I_{ripple} in the continuous-conduction mode at $I_{\text{LOAD}} = 4\text{A}$ for $V_{\text{IN}} = 5\text{V}$ and $V_{\text{IN}} = 8\text{V}$.

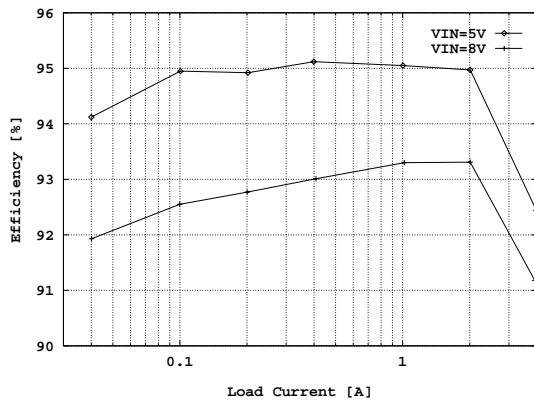


Figure 11: Efficiency of the experimental converter as a function of the load current for $V_{\text{IN}} = 5\text{V}$ and $V_{\text{IN}} = 8\text{V}$.

and with the load current from 40mA to 4A. The output voltage stays within $\pm 1\%$ of the nominal value for all input voltages and all loads in the specified range, including large-signal 100:1 load transients. These characteristics are particularly important for battery-powered systems with power management.

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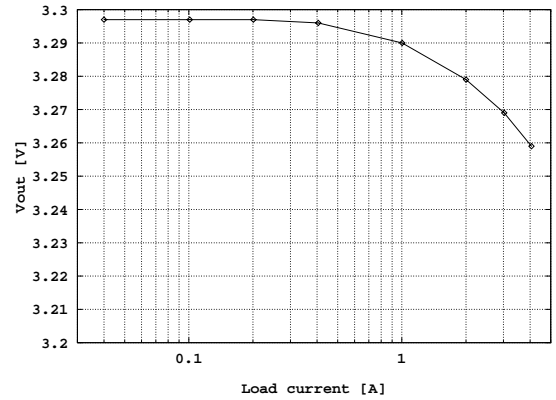


Figure 12: DC load regulation in the experimental converter.

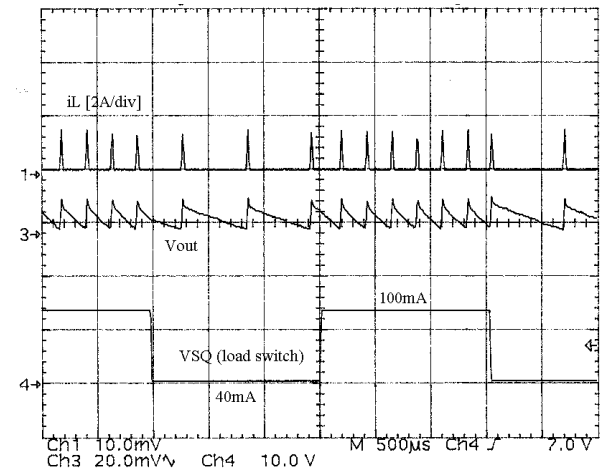


Figure 13: 40mA-to-100mA load transient response in the experimental converter at $V_{\text{IN}} = 5\text{V}$. Top to bottom: inductor current i_L , output voltage v_{OUT} , load switch control V_{SQ} .

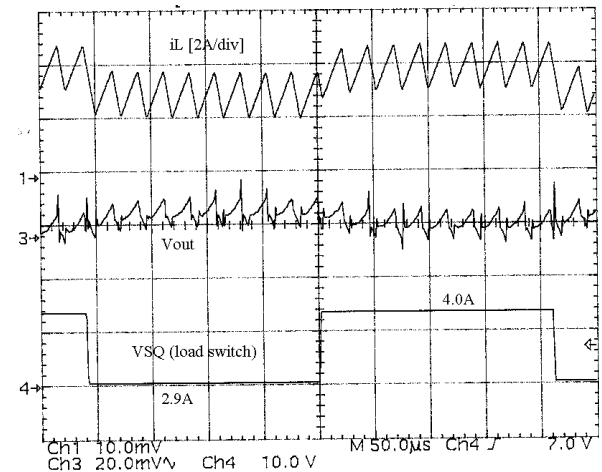


Figure 14: 2.9A-to-4A load transient response in the experimental converter at $V_{\text{IN}} = 5\text{V}$. Top to bottom: inductor current i_L , output voltage v_{OUT} , load switch control V_{SQ} .