Manish Vachharajani

Curriculum Vitae

Contact Information

Department of Electrical and Computer Engineering
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Education

Princeton University
Ph.D. in Electrical Engineering, November 2004
M.A. in Electrical Engineering, May 2004

Rutgers, The State University of New Jersey, New Brunswick, NJ
B.S. in Electrical and Computer Engineering, Highest Honors, May 1998

Experience

Founder and Chief Technology Officer (CTO), October 2008 to Present
LineRate Systems, Boulder, CO

Assistant Professor (on leave), August 2004 to Present
Department of Electrical and Computer Engineering, *University of Colorado*, Boulder, CO

Recognition

- Best Paper Award for "Compiler Optimization-Space Exploration" at the First Annual ACM/IEEE International Symposium on Code Generation and Optimization, March 2003.
- Best Student Paper Award for "Microarchitectural Exploration with Liberty" at the 35th Annual ACM/IEEE International Symposium on Microarchitecture, November 2002.
- Intel Foundation Graduate Fellowship, 2002-2003.

Professional Activities

Technical Program Committees

- The 24th International Conference on VLSI Design (VLSI), Architecture Track Subcommittee, 2010
- The ACM/IEEE Symposium on Architectures for Networking and Communications Systems, 2009
- The 23rd International Conference on VLSI Design (VLSI), Architecture Track Subcommittee, 2009
- The 2009 International Symposium on Microarchitecture (MICRO), 2009
- The 2009 International Symposium on Code Generation and Optimization (CGO), 2009
- The 4th Symposium on Architectures for Networking and Communications Systems (ANCS), 2008.
- The 3rd Symposium on Architectures for Networking and Communications Systems (ANCS), 2007.
- 2007 Workshop on Software Tools for Multi-Core Systems (STMCS), 2007.
- 2007 Workshop on Computer Architecture Education (WCAE), 2007.

Conference Organizing Committees

- Co-Chair, The 2008 Workshop on Explicitly Parallel Instruction Computing (EPIC), April 2008.
- Principal Organizer, Fall 2007 Front-Range Architecture, Compilers, Tools, and Langagues Regional Workshop (FRACTAL), 2007.
- Submissions Chair, The 39th Annual International Symposium on Microarchitecture (MICRO), 2006.
- Web Chair, The 4th Annual International Symposium on Code Generation and Optimization (CGO), 2006.

Reviews

- Journals: ACM Transaction on Architecture and Code Optimization (TACO), ACM Transactions on Computer Systems (TOCS), Journal of Instruction Level Parallelism (JILP), IEEE Transactions on CAD (TCAD), IEEE Transactions on VLSI (TVLSI)
- Conferences: ASPLOS, ANCS, DAC, CGO, MICRO, ISCA, CASES, HPCA, LCTES, PACT, PLDI, VLSI

Tutorials

- "Using The Liberty Simulation Environment with emphasis on validated OS-level simulation," presented at the 11th International Conference on Architectural Support for Programming Languages and Operating Systems in Boston, MA, October 2004.
- "The Liberty Simulation Environment, Version 1.0," presented at the 36th International Symposium on Microarchitecture in San Diego, CA, December 2003.
- "Architectural Exploration with Liberty," presented at the International Symposium on Microarchitecture in Austin, TX, December 2001.

Invited Talks

- "FastForward: A Cache Optimized Concurrent Lock-free Queue" presented at Google, June 2008.
- "FastForward: A Cache Optimized Concurrent Lock-free Queue" presented at Intel, March 2008.
- "Recognizing Opportunities for Thread-level Parallelism Through Trace Analysis" presented at Google, March 2007.
- "Finding Large-scale Parallelism" presented at Hewlett Packard, 2005.

University Service

- ECE Ad-hoc Committee on Undergraduate Laboratories, 2006-2008
- Chair of the Computer Engineering Prelims Committee, 2006

Teaching

- ECEN 5023: Programming Non-traditional Multiprocessors (2 semesters)
- ECEN 5553: Parallel Processing (3 semesters)
- ECEN 4593: Computer Organization (3 semesters)
- ECEN 5593: Advanced Computer Architecture (4 semesters)
- ECEN 5003-001: Evaluating Processor Microarchitectures

Publications

Refereed Journal Publications

[1] Zheng Li, Moustafa Mohammed, Xi Chen, Eric Dudley, Ke Meng, Li Shang, Alan Mickelson, Russ Joseph, Manish Vachharajani, Brian Schwartz, and Yihe Sun, "Reliability Modeling and Management of Nanophotonic On-Chip Networks," to appear in *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, 2011. (15 pages)

[2] John Michalakes and Manish Vachharajani, "GPU Acceleration of Numerical Weather Prediction," in *Parallel Programming Letters (PPL)*, December 2008. Invited. (18 pages)

[3] Graham D. Price and Manish Vachharajani, "A Case for Compressing Traces with BDDs," in *IEEE Computer Architecture Letters (CAL)*, December 2006. (4 pages)

[4] Manish Vachharajani, Neil Vachharajani, David A. Penry, Jason A. Blome, Sharad Malik, and David I. August, "The Liberty Simulation Environment: A Deliberate Approach to High-Level System Modeling," in *ACM Transactions on Computer Systems (TOCS)*, pp. 211-249, August 2006.

[5] David I. August, Sharad Malik, Li-Shiuan Peh, Vijay Pai, Manish Vachharajani, and Paul Willmann, "Achieving Structural and Composable Modeling of Complex Systems," in *The International Journal of Parallel Programming (IJPP)*, pp. 81-101, June 2005. Invited.

[6] Spyridon Triantafyllis, Manish Vachharajani, and David I. August, "Compiler Optimization-Space Exploration," in *The Journal of Instruction-level Parallelism (JILP)*, February 2005. (12 pages)

[7] Manish Vachharajani, Neil Vachharajani, David A. Penry, Jason Blome, and David I. August, "The Liberty Simulation Environment, Version 1.0," in *Performance Evaluation Review: Special Issue on Tools for Architecture Research (PER)*, pp. 19-24, March 2004. Invited.

Refereed Conference Publications

[8] Moustafa Mohamed, Zheng Li, Xi Chen, Li Shang, Alan Mickelson, Manish Vachharajani, and Yihe Sun, "Power-Efficient Variation-Aware Photonic On-Chip Network Management," in *The ACM Internatioal Symposium on Low Power Electronics and Design (ISLPED)*, August 2010. (4 pages)
Nominated For Best Paper Award

[9] Justin E. Gottschlich, Manish Vachharajani, and Jeremy G. Siek, " An Efficient Software Transactional Memory Using Commit-Time Invalidation," in *Proceedings of the 2010 ACM/IEEE International Symposium on Code Generation and Optimization (CGO'10)* , pp. 101-110, April 2010. [Accept Rate: 39% (29/74)]
Best Presentation Award

[10] Graham D. Price and Manish Vachharajani, " Large Program Trace Analysis and Compression with ZDDs," in *Proceedings of the 2010 ACM/IEEE International Symposium on Code Generation and Optimization (CGO'10)* , pp. 32-41, April 2010. [Accept Rate: 39% (29/74)]

[11] John C. Linford, John Michalakes, Manish Vachharajani, and Adrian Sandu, "Multi-core Acceleration of Chemical Kinetics for Simulation and Prediction," in *Proceedings of the International Conference on High Performance Computing, Networking, Storage, and Analysis (SC)*, November 2009. (11 pages)

[12] Zheng Li, Alan Mickelson, Li Shang, Manish Vachharajani, Dejan Filipovic, Wounjhang Park, and Y. Sun, "A High-performance Low-power Nanophotonic On-chip Network," in *The ACM Internatioal Symposium on Low Power Electronics and Design (ISLPED)*, August 2009. (4 pages) [Accept Rate: 24%

[13] Zheng Li, Alan Mickelson, Li Shang, Manish Vachharajani, Dejan Filipovic, Wounjhang Park, and Y. Sun, "Spectrum: A Hybrid Nanophotonic-electric On-chip Network," in *The 46th Annual IEEE Design Automation Conference (DAC)*, July 2009. (6 pages) [Accept Rate: 21%

[14] Graham D. Price, John Giacomoni, and Manish Vachharajani, "Visualizing Potential Parallelism in Sequential Programs," in *The 17th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, October 2008. (10 pages)

[15] Jeremy G. Siek and Manish Vachharajani, "Gradual Typing with Unification-based Inference," in *Proceedings of the 2008 Dynamic Languages Symposium (DLS)*, July 2008. (12 pages) [Accept Rate: 40%

[16] John Giacomoni, Tipp Moseley, and Manish Vachharajani, "FastForward for Efficient Pipeline Parallelism: A Cache-Optimized Concurrent Lock-Free Queue," in *Proceedings of the 13th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP)*, February 2008. (10 pages) [Accept Rate: 24% (25/102)]

[17] John Giacomoni, John K. Bennet, Antonio Carzaniga, Douglas C. Sicker, Manish Vachharajani, and Alexander L. Wolf, "Frame Shared Memory: Line-Rate Networking on Commodity Hardware," in *Proceedings of the 2007 ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS)*, pp. 27-36, December 2007. [Accept Rate: 28% (20/70)]

[18] John Giacomoni, Tipp Moseley, and Manish Vachharajani, "FastForward for Efficient Pipeline Parallelism," in *Proceedings of the 16th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2007. (1 page) [Poster.]

[19] Neil Vachharajani, Matthew J. Bridges, Jonathan Chang, Ram Rangan, Guilherme Ottoni, Jason A. Blome, George A. Reis, Manish Vachharajani, and David I. August, "RIFLE: An Architectural Framework for User-Centric Information-Flow Security," in *Proceedings of the 37th International Symposium on Microarchitecture (MICRO)*, pp. 243-254, December 2004. [Accept Rate: 18% (29/158)]

[20] Manish Vachharajani, Neil Vachharajani, Sharad Malik, and David I. August, "Facilitating Reuse in Hardware Models with Enhanced Type Inference," in *The IEEE/ACM/IFIP Second International Conference on Hardware/Software Codesign and System Synthesis (ISSS)*, pp. 86-91, September 2004. [Accept Rate: 24% (39/159)]

[21] Ram Rangan, Neil Vachharajani, Manish Vachharajani, and David I. August, "Decoupled Software Pipelining with the Synchronization Array," in *Proceedings of the 13th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, pp. 177-188, September 2004. [Accept Rate: 18% (23/122)]
Highest ranked paper by the anonymous reviewers.

[22] Manish Vachharajani, Neil Vachharajani, and David I. August, "The Liberty Structural Specification Language: A High-Level Modeling Language for Component Reuse," in *Proceedings of the 2004 ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pp. 195-206, June 2004. [Accept Rate: 19% (25/128)]

[23] Spyridon Triantafyllis, Manish Vachharajani, Neil Vachharajani, and David I. August, "Compiler Optimization-Space Exploration," in *Proceedings of the 2003 International Symposium on Code Generation and Optimization (CGO)*, pp. 204-215, March 2003. [Accept Rate: 35% (29/82)]
Winner Best Paper Award.

[24] Manish Vachharajani, Neil Vachharajani, David A. Penry, Jason A. Blome, and David I. August, "Microarchitectural Exploration with Liberty," in *Proceedings of the 35th International Symposium on Microarchitecture (MICRO)*, pp. 271-282, November 2002. [Accept Rate: 24% (36/150)]
Winner Best Student Paper Award.

[25] Subramanian Rajagopalan, Manish Vachharajani, and Sharad Malik, "Handling Irregular ILP Within Conventional VLIW Schedulers Using Artificial Resource Constraints," in *Proceedings of the International Conference on Compilers and Synthesis for Embedded Systems*, pp. 157-164, November 2000.

[26] Xiao Yang, Manish Vachharajani, and Ruby B. Lee, "Fast Subword Permutation Instructions Based on Butterfly Networks," in *Proceedings of SPIE, Media Processor 2000*, pp. 80-86, January 2000.

Refereed Workshop Publications

[27] Justin E. Gottschlich, Jeremy G. Siek, and Manish Vachharajani, "Proving Conflict Serializability for Full Invalidation," in *Proceedings of the 2nd Workshop on the Theory of Transactional Memory (WTTM)* , September 2010.

[28] Justin E. Gottschlich, Jeremy G. Siek, Manish Vachharajani, Dwight Y. Winkler, and Daniel A. Connors, " An Efficient Lock-Aware Transactional Memory Implementation," in *Proceedings of the 2009 ACM International Workshop on the Implementation, Compilation, Optimization of Object-Oriented Languages, Programs and Systems (ICOOOLPS). In conjunction with ECOOP.* , July 2009.

[29] John Michalakes and Manish Vachharajani, "GPU Acceleration of Numerical Weather Prediction," in *2008 Workshop on Large-Scale Parallel Processing (LSPP)*, April 2008. (8 pages) [Accept Rate: 39% (11/28)]

[30] John Giacomoni and Manish Vachharajani, "Operating System Support for Pipeline Parallelism on Multicore Architectures," in *2007 Workshop on Operating Systems Support for Heterogeneous Multicore Architectures (OSHMA)*, September 2007. (8 pages)

[31] John Giacomoni, Tipp Moseley, Graham Price, Brian Bushnell, Manish Vachahrajani, and Dirk Grunwald, "Toward a Toolchain for Pipeline Parallel Programming on CMPs," in *Proceedings of the 2007 Workshop on Software Tools for Multicore Systems (STMCS)*, March 2007. (4 pages)

[32] Budyanto Himawan and Manish Vachharajani, "Deconstructing Hardware Usage for General Purpose Computation on GPUs (GPGPU)," in *Proceedings of the 2006 Workshop on Duplicating, Debunking, and Deconstructing (WDDD)*, June 2006. (12 pages)

[33] Neil Vachharajani, Matthew Iyer, Chinmay Ashok, Manish Vachharajani, David I. August, and Daniel A. Connors, "Chip Multi-Processor Scalability for Single-Threaded Applications," in *Proceedings of the 2005 Workshop on Design, Architecture and Simulation of Chip Multi-Processors (dasCMP)*, pp. 44-53, November 2005.

[34] David A. Penry, Manish Vachharajani, and David I. August, "Rapid Development of Flexible Validated Processor Models," in *Proceedings of the Workshop on Modeling, Benchmarking, and Simulation (MoBS)*, pp. 21-30, June 2005. [Accept Rate: 45% (10/22)]

[35] Matthew Iyer, Chinmay Ashok, Joshua Stone, Neil Vachharajani, Daniel A. Connors, and Manish Vachharajani, "Finding Parallelism for Future EPIC Machines," in *Proceedings of the Fourth Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology (EPIC)*, March 2005. (13 pages)

[36] Jason Blome, Manish Vachharajani, Neil Vachharajani, and David I. August, "The Liberty Simulation Environment as a Pedagogical Tool," in *Proceedings of the Workshop on Computer Architecture Education (WCAE)*, June 2003. (7 pages)

[37] Spyridon Triantafyllis, Manish Vachharajani, and David I. August, "Procedure Boundary Elimination for EPIC Compilers," in *Proceedings of the Second Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology (EPIC)*, November 2002. (7 pages)

[38] Wei Qin, Subramanian Rajagopalan, Manish Vachharajani, Hangsheng Wang, Xinping Zhu, David I. August, Kurt Keutzer, Sharad Malik, and Li-Shiuan Peh, "Design Tools for Application Specific Embedded Processors," in *Proceedings of the Second International Workshop on Embedded Software, Lecture Notes in Computer Science (EMSOFT)*, pp. 319-333, October 2002. Invited.

Technical Reports

[39] Jeremy Siek and Manish Vachharajani, "Gradual Typing with Unification-based Inference," *University of Colorado Technical Report CU-CS-1039-08*, February 2008.

[40] John Giacomoni, Tipp Moseley, and Manish Vachharajani, "FastForward for Efficient Pipeline Parallelism," *University of Colorado Technical Report CU-CS-1028-07*, April 2007.

[41] John Giacomoni and Manish Vachharajani, "Harnessing Chip-Multiprocessors with Concurrent Threaded Pipelines," *University of Colorado Technical Report CU-CS-1024-07*, January 2007.

[42] John Giacomoni, Tipp Moseley, and Manish Vachharajani, "FastForward for Concurrent Threaded Pipelines," *University of Colorado Technical Report CU-CS-1023-07*, January 2007.

[43] John Giacomoni, John K. Bennet, Antonio Carzaniga, Manish Vachharajani, and Alexander L. Wolf, "FShm: High-rate Frame Manipulation in Kernel and User-Space," *University of Colorado Technical Report CU-CS-1015-06*, October 2006.

[44] David A. Penry, Manish Vachharajani, and David I. August, "Rapid Development of Flexible Validated Processor Models," *Liberty Research Group Technical Report 04-03*, November 2004.

[45] Manish Vachharajani, Neil Vachharajani, David A. Penry, Jason A. Blome, Sharad Malik, and David I. August, "The Liberty Simulation Environment: A Deliberate Approach to High-Level System Modeling," *Liberty Research Group Technical Report 04-02*, March 2004.

[46] Manish Vachharajani and David I. August, "A Study of the Clarity of Functionally and Structurally Composed High-level Simulation Models," *Liberty Research Group Technical Report 04-01*, January 2004.

[47] Manish Vachharajani, Neil Vachharajani, and David I. August, "A Comparison of Reuse in Object-oriented Programming and Structural Modeling Systems," *Liberty Research Group Technical Report 03-01*, October 2003.

Other Publications

[48] Manish Vachharajani, "Microarchitecture Modeling for Design-space Exploration," Ph.D. Dissertation, Princeton University, November 2004.

Released Software

[49] Manish Vachharajani, David A. Penry, Neil Vachharajani, Jason A. Blome, and David I. August, "Liberty Simulation Environment, Version 1.0," Released in December 2003, available at `http://liberty.princeton.edu/Software/LSE`.

Pending Patents

[50] John Giacomoni and Manish Vachharajani, "Method and Apparatus for Efficient Pipeline Parallelism Using Frame Shared Memory,", Filed April 21, 2008

[51] John Giacomoni and Manish Vachharajani, "Efficient Point-To-Point Enqueue and Dequeue Communications,", Filed April 21, 2008