

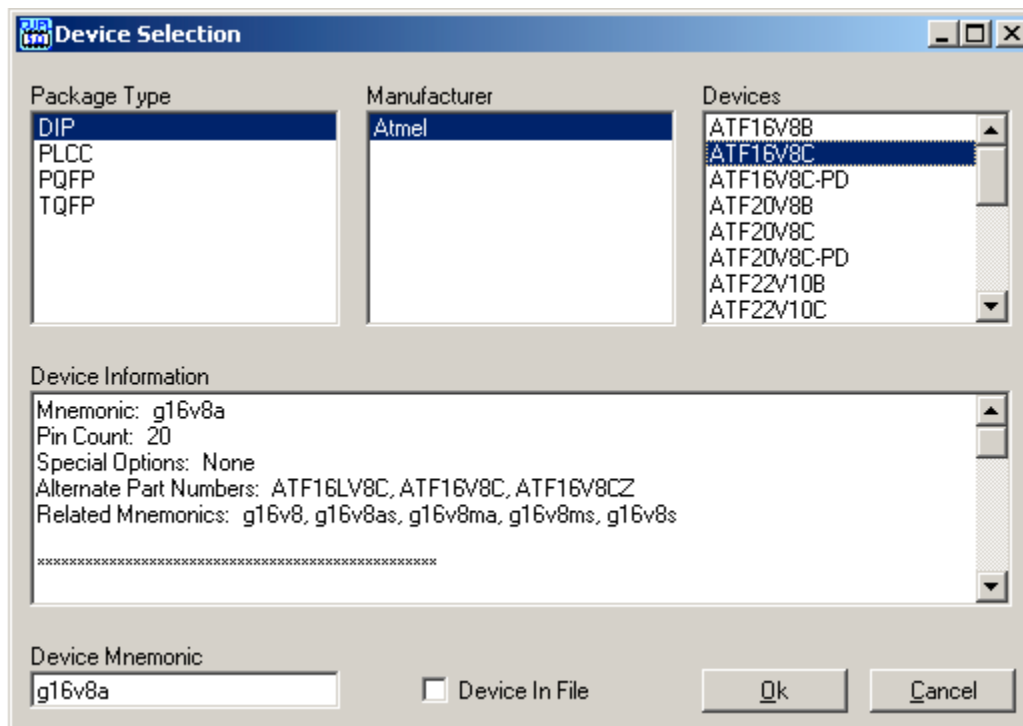
Programming the Atmel ATF16V8C SPLD

A) Generating JEDEC file for SPLD

SPLD devices require a JEDEC file in order to program the logic functions. To generate a JEDEC file from WinCUPL, please follow the following steps.

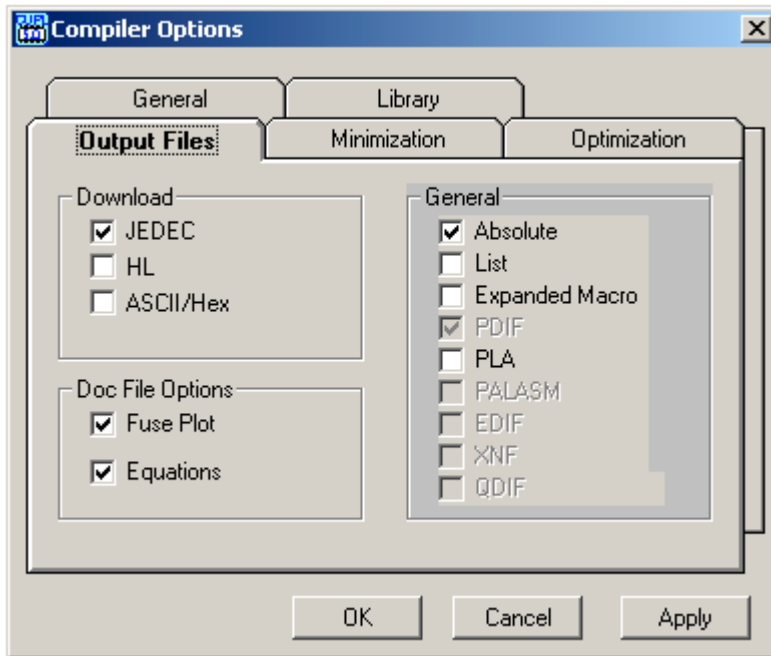
Step 1:

- Open Atmel WinCUPL.
- Create a new project
- Develop logic in the *.PLD file (refer to tutorials on course website to write .PLD files)
- Go to Options->Devices to select device.
Select Atmel ATF16v8C device and uncheck the box “Device In File” at the bottom of the window as shown in following figure.
- Click Ok

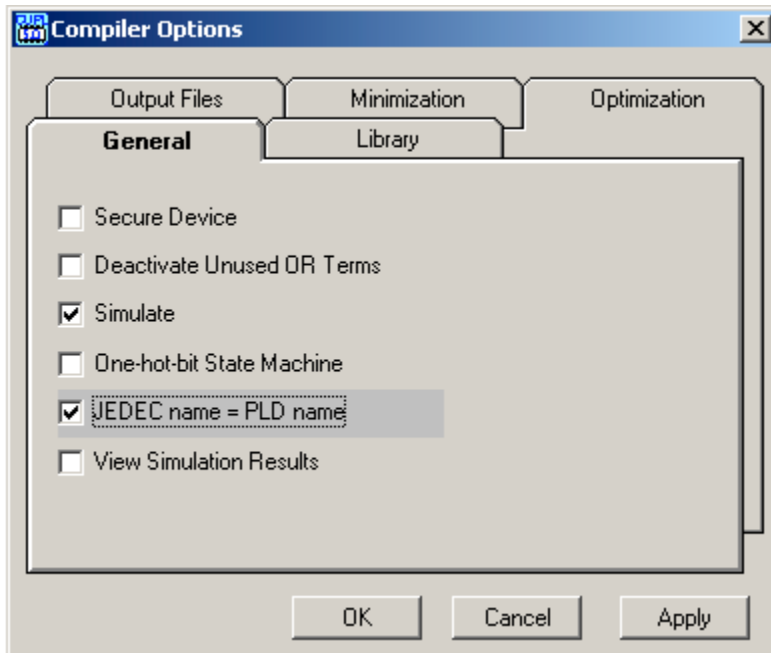


Step 2:

- Go to Options->Compiler to select compiler options.
- Under “Output Files” tab, check the JEDEC box and also check the “Fuse Plot” and “Equations” options as shown in following figure.



- Under the General tab, select “JEDEC Name = PLD Name” as shown below.

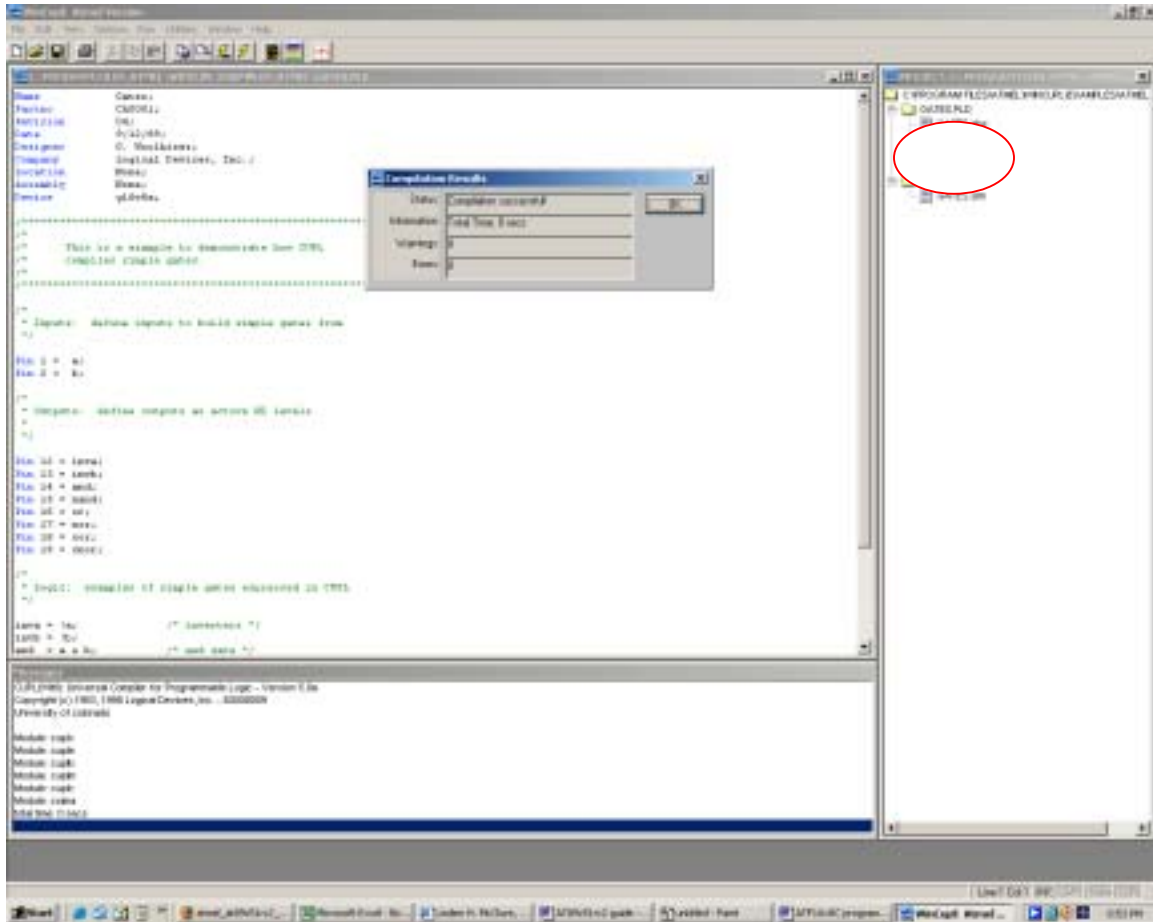


- Click Apply and then OK.

Step 3: Compile PLD file

Go to Run - > Device Dependent Compile Or Press F9

Now if the PLD file is error free, then the compilation process will generate a *.jed file. The *.jed file can be seen in the Project window (shown in the circle below).

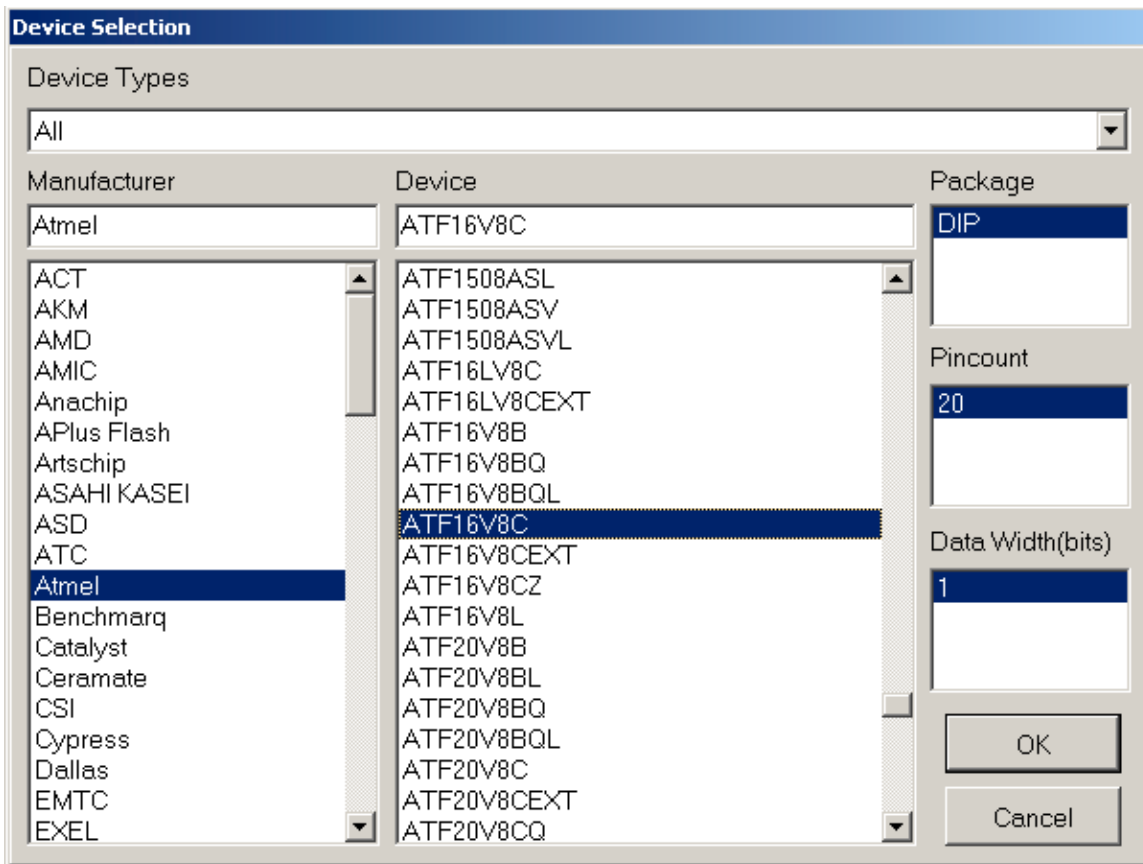


B) Programming SPLD using *.jed file

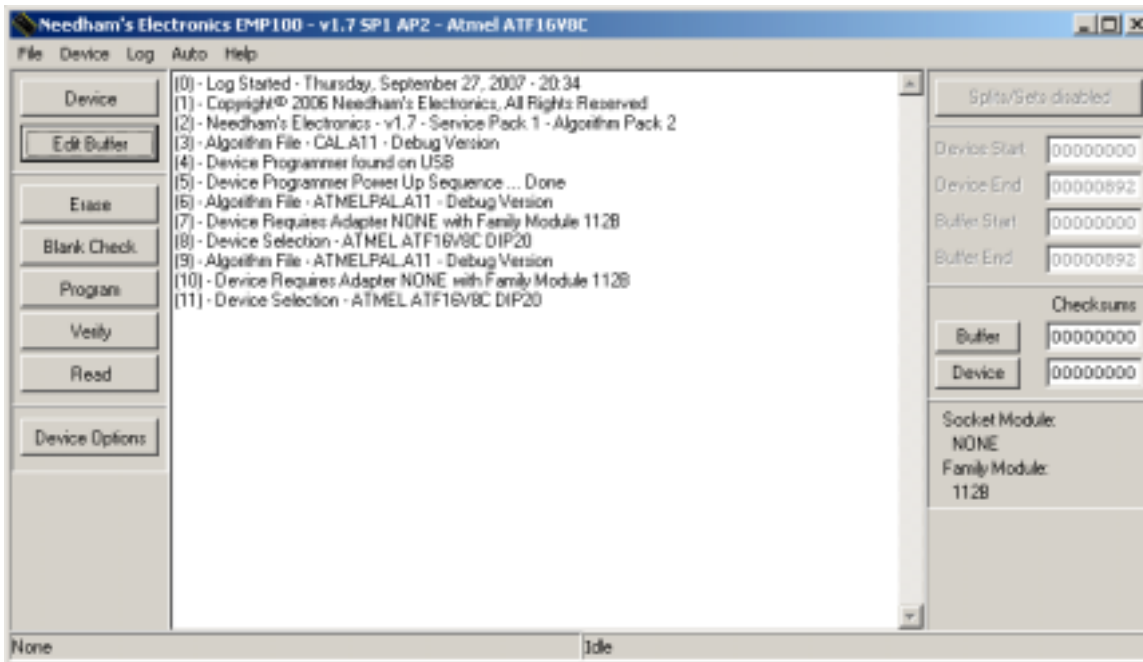
Step 1 : Make sure the correct family module (112B) is inserted into the NEI EMP-100 programmer. Other family modules are taped to the bottom side of the EMP-100 programmer.

Step 2 : Open nei->EMP100 programmer software

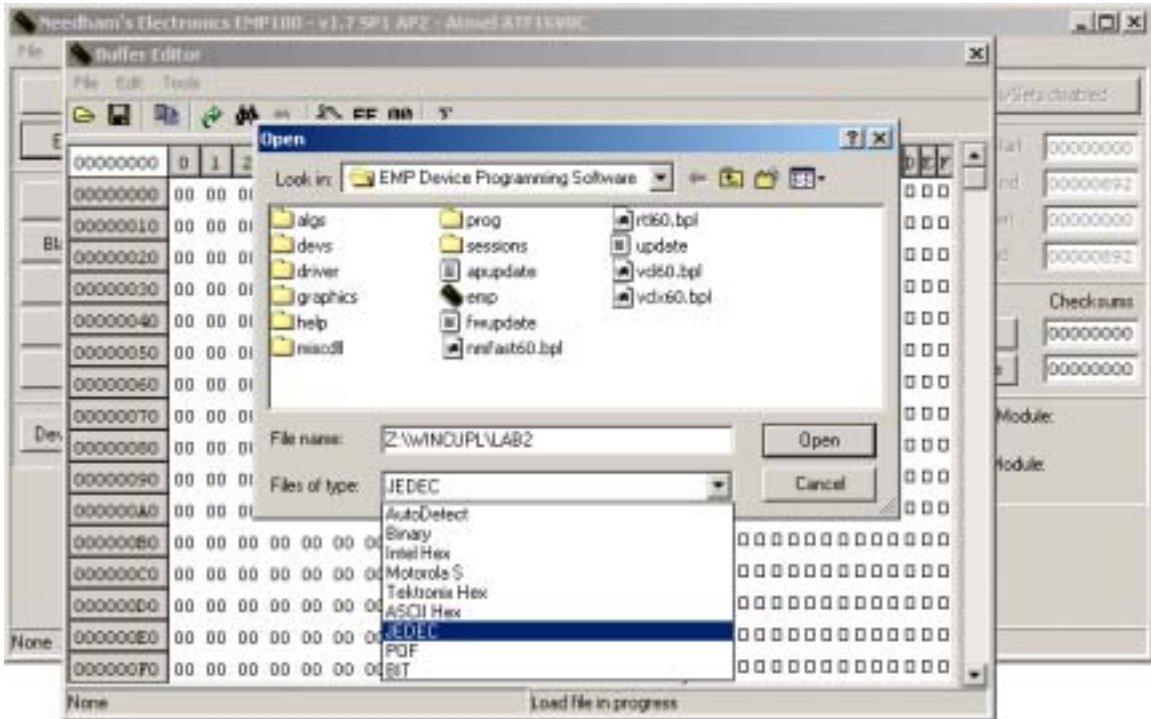
Step 3 : Select Device



Step 4: After selecting device, press Edit buffer to load the *.jed file into the buffer



Step 5: In Buffer Editor, open a *.jed file to load file into buffer, and then close the Buffer Editor window.



Step 6: Erase the IC if it is not Blank.

Step 7: Click Program to program the device.