LogicPort Logic Analyzer Notes

For in-depth information, please refer to the LogicPort in-program help.

There are two main views in the LogicPort program.

State List

- Use this tab to display a trace in listing format. This is very useful for state mode analysis and for examining sequences on the bus.

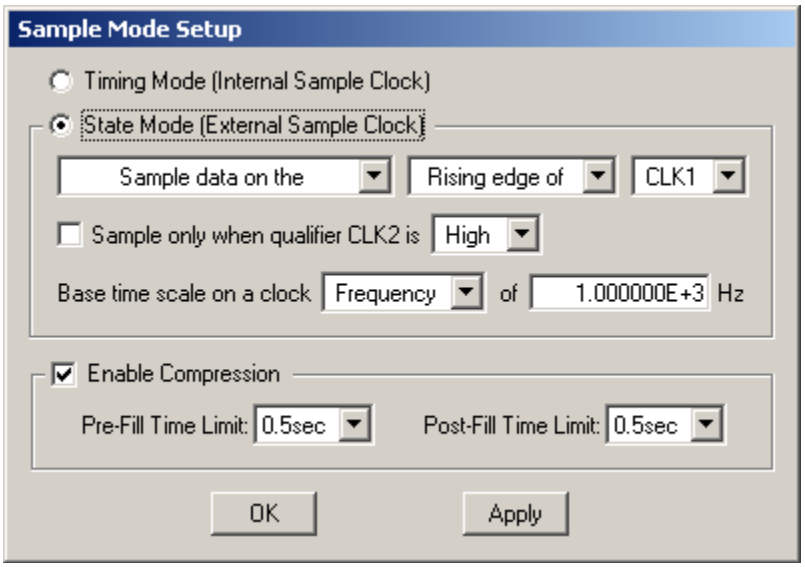
Waveforms

- Use this tab to display a trace as a waveform. Relative timing between signal edges can be measured with the cursors.
- Display a multi-signal label as a bus, rather than multiple individual signals. For example, display ADDR or DATA as a bus rather than separate signals ADDR[0], ADDR[1], ...
- Adjust the waveform view by changing the zoom options in the View menu or with zoom buttons.
- When using timing mode, set the Sample Rate to >100 MHz for the most accurate measurements.
- The LogicPort software allows up to six cursors which can be placed by right-clicking on the waveform view and selecting which cursor to place at that location.
- Click and drag a cursor to where you want it. The cursor will snap to the closest sampling point.
- Measurements between cursors and the trigger are available in the status bar at the bottom of the window.
- Measurements can be configured by right clicking on the status bar.

The following sections describe how to change the behavior of the LogicPort Logic Analyzer software.

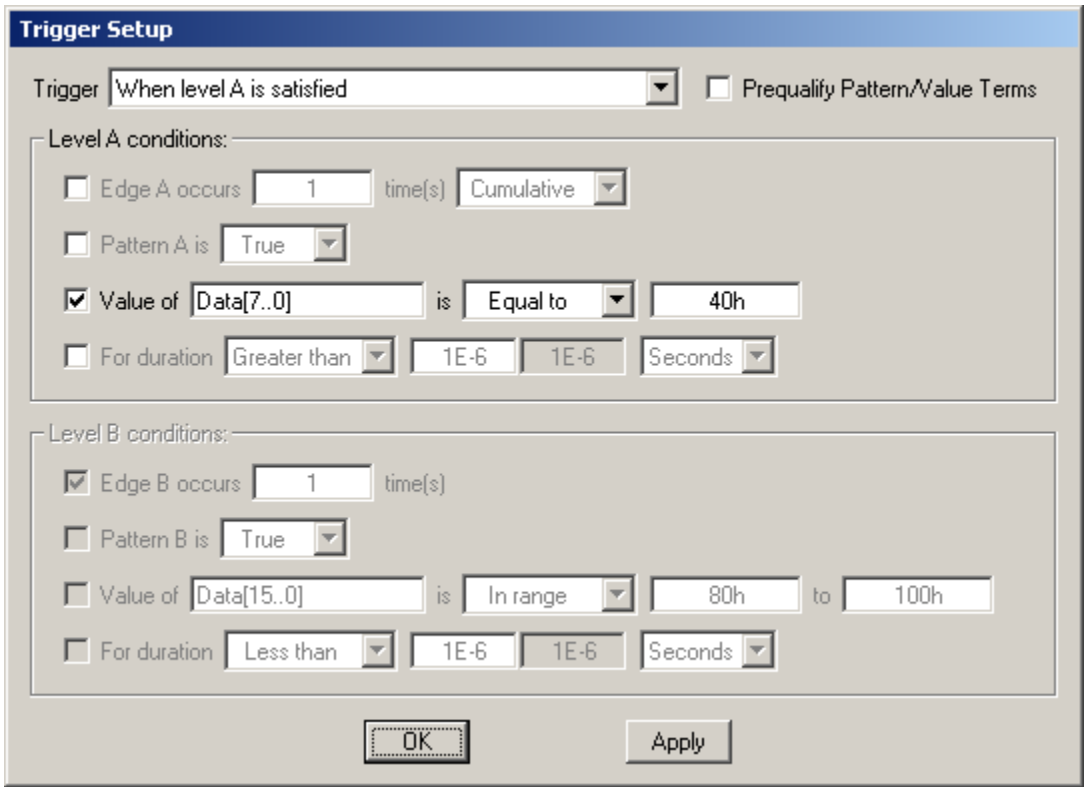
Sample Mode

- To access the Sample Mode Setup, go to Setup > Sample Mode… or the button with a square wave with three downward pointing blue arrows.
- **Timing Mode:** LA uses an internal clock for sampling the inputs. The CLK lines can be left unconnected.
- **State Mode:** LA uses a CLK line to sampling the inputs. Typical choices for the CLK input are the /PSEN, /READ, or ALE signals.



Trigger

- The Trigger dialog is located in the Setup > Trigger… menu or button with a red T with square waves in the background.
- Use this dialog to set up the trigger for when the logic analyzer should display captured information. You can configure a specific data pattern or value or specific clock edges at which point the trigger should occur.
- To trigger on an edge, select the Edge A or Edge B checkboxes.
- Which signal(s) and the type of edge are controlled in the Waveforms view, not the Trigger Setup dialog. Click the Edge A or B column in the signal row to cycle between positive, negative or either edge trigger modes.
- To trigger on a specific pattern, specify the pattern in the Pattern A or B column or use the
- To trigger on a specific value, specify the value in the trigger pop-up. The Value trigger is easier to use than the Pattern if you want to trigger on a bus being a certain value. For example, Data[7..0] = 50h.
- Any combination of these triggers is also possible. Be sure to select only the options you wish to have enabled, typically Edge A or Value.

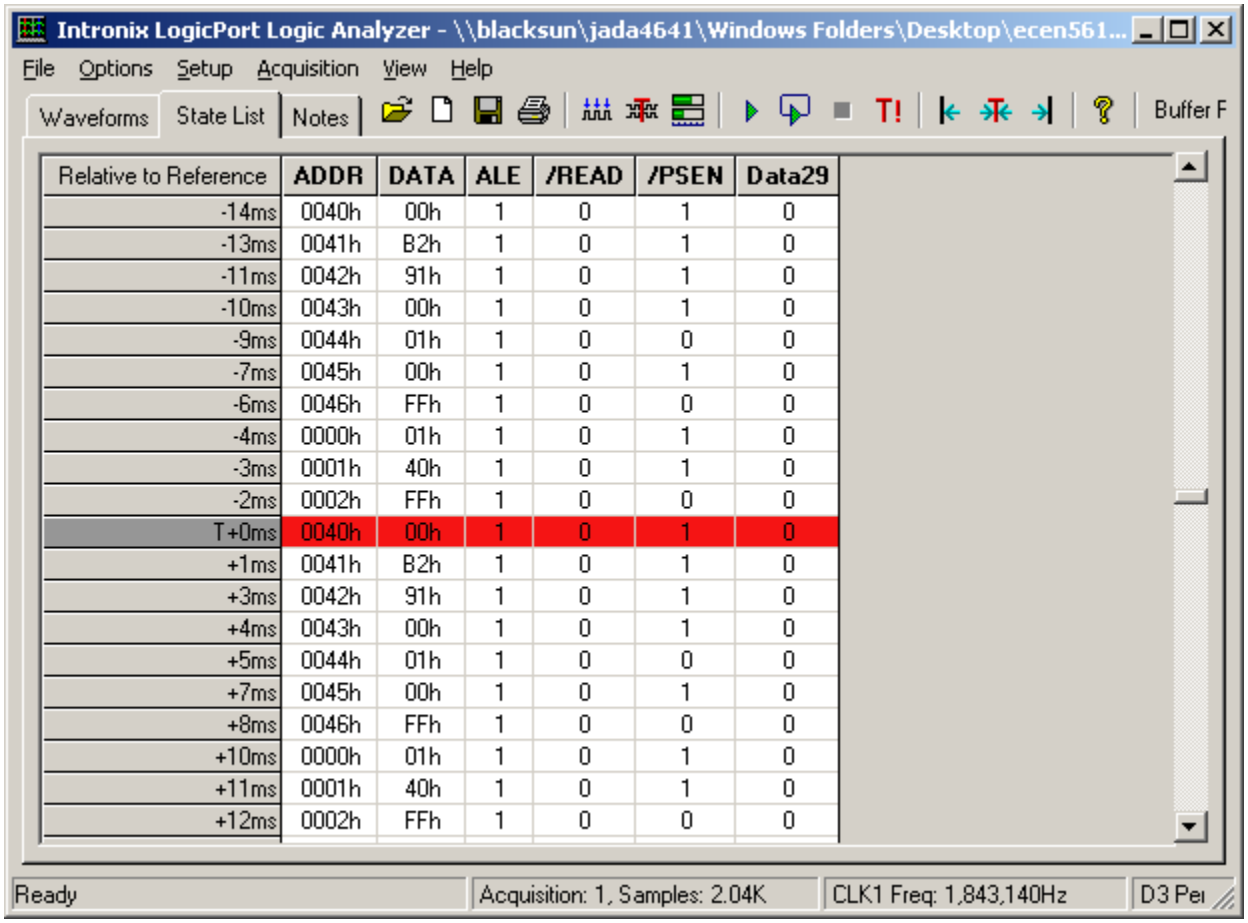


Signal Format

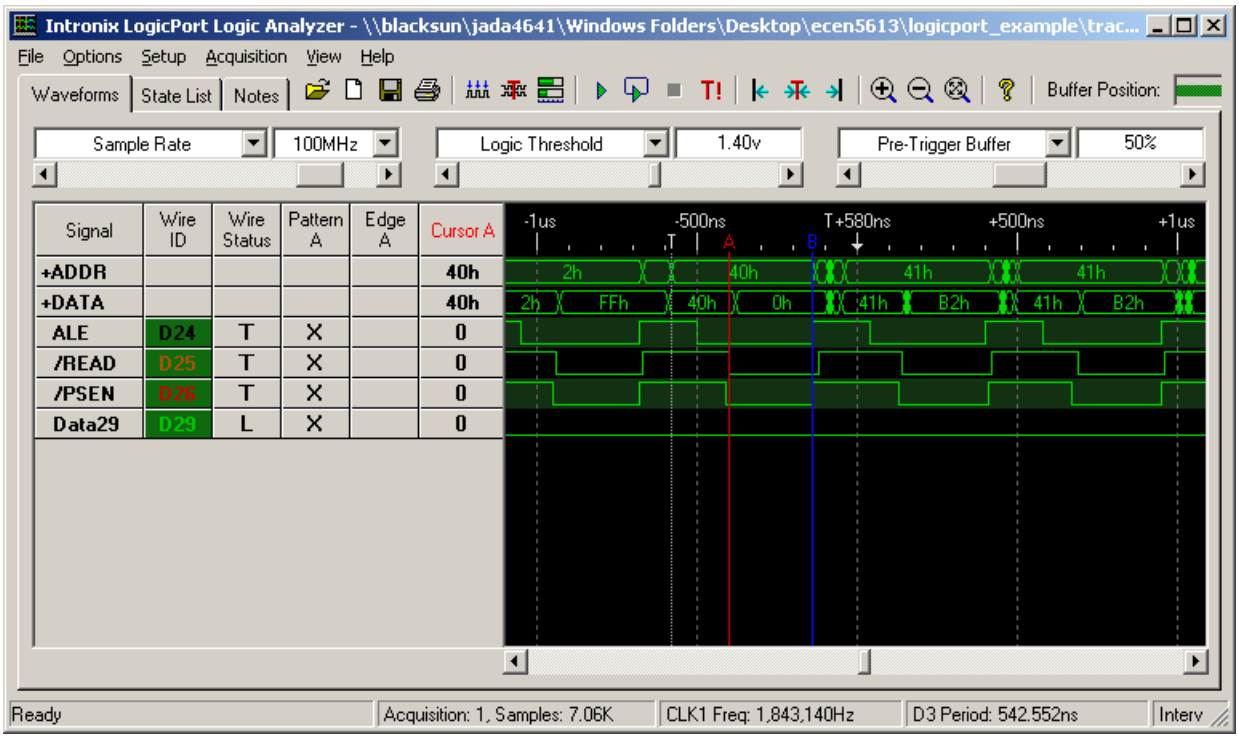
- Signals can be renamed in the Setup > Signal Names… menu item.
- Signals can be grouped in the Setup > Groups… menu item. The Create… button will bring up a dialog to select which signals are in the group and to name the group.
- You can assign names to a single signal or to groups of signals. For instance, you can have one label called ADDR which identifies address lines A15:A0. You can have another label which identifies data lines D7:D0.
- To add, modify or remove signals from the Waveforms and State List views, right click on the gray area on the left side of the screen and select the your desired option.
- Interpreters for I2C, SPI, RS232 and CAN are accessed in the Setup > Interpreters… menu item.

LogicPort Logic Analyzer Example – C501 Bus Cycles

```
0000                    1  *       ECEN 5613
0000                    2  *       Embedded System Design
0000                    3  *       Logic Analyzer Example
0000                    4  *
0000                    5
0000                    6          ORG     $0000   Reset Vector
0000  01 40             7  Start   AJMP    CBIT    Jump to code
0002                    8
0040                    9          ORG     $0040   Code starts here
0040                   10
0040                   11
0040  00               12  CBIT    NOP             Do Nothing
0041  B2 91            13          CPL P1.1        Complement port pin P1.1
0043  00               14          NOP             Do Nothing
0044  01 00            15          AJMP Start      Jump back to Start
```



Relative to Reference	ADDR	DATA	ALE	/READ	/PSEN	Data29
-14ms	0040h	00h	1	0	1	0
-13ms	0041h	B2h	1	0	1	0
-11ms	0042h	91h	1	0	1	0
-10ms	0043h	00h	1	0	1	0
-9ms	0044h	01h	1	0	0	0
-7ms	0045h	00h	1	0	1	0
-6ms	0046h	FFh	1	0	0	0
-4ms	0000h	01h	1	0	1	0
-3ms	0001h	40h	1	0	1	0
-2ms	0002h	FFh	1	0	0	0
T+0ms	0040h	00h	1	0	1	0
+1ms	0041h	B2h	1	0	1	0
+3ms	0042h	91h	1	0	1	0
+4ms	0043h	00h	1	0	1	0
+5ms	0044h	01h	1	0	0	0
+7ms	0045h	00h	1	0	1	0
+8ms	0046h	FFh	1	0	0	0
+10ms	0000h	01h	1	0	1	0
+11ms	0001h	40h	1	0	1	0
+12ms	0002h	FFh	1	0	0	0


Intronix LogicPort Logic Analyzer - \\blacksun\jada4641\Windows Folders\Desktop\ecen5613\logicport_example\trac...
File Options Setup Acquisition View Help
Waveforms State List Notes
Buffer Position:
Sample Rate 100MHz
Logic Threshold 1.40v
Pre-Trigger Buffer 50%
Signal Wire ID Wire Status Pattern A Edge A Cursor A
+ADDR 40h
+DATA 40h
ALE D24 T X 0
/READ D25 T X 0
/PSEN D26 T X 0
Data29 D29 L X 0
-1us -500ns T+580ns +500ns +1us
2h 40h 41h 41h
2h FFh 40h 0h 41h B2h 41h B2h
Ready
Acquisition: 1, Samples: 7.06K
CLK1 Freq: 1,843,140Hz
D3 Period: 542.552ns
Interv