Understanding Timing Diagrams and the C501 Data Sheet

Overview of Timing

Integrated circuit manufacturers provide timing specifications for their chips. The timing specifications dictate requirements on how the IC is designed into a circuit. Due to variations in the semiconductor manufacturing process, individual chips have different absolute timing characteristics. Timing specifications are determined in part by design parameters and in part by laboratory testing of a statistically significant sampling of ICs. Chip manufacturers test their semiconductors and for each timing parameter, determine the maximum and minimum timing limits which can be guaranteed for a variety of chips manufactured on different wafers at different times in potentially different IC fabrication facilities.

The C501 processor used in class is the SAB-C501G-1RP, which is a 5V processor in a 40-pin P-DIP (Plastic Dual In-line Package), capable of running at up to 12 MHz, at temperatures from 0 to 70 degrees Celsius. This chip has 8KB of mask programmable ROM, which we disable by wiring the /EA line low. When referring to the timing diagrams and tables in the C501 data sheet, refer to the set of tables with AC characteristics for the C501-1R. For any clock speed other than 12 MHz, the value for each timing parameter must be calculated, based on the value of t_{CLCL}, which is the clock period. For an 11.0592 MHz crystal frequency, t_{CLCL}=90.42ns.

Setup Time (t_{SU}):The minimum time that data must be held valid at the receiver input before the clock edge arrives at the receiver.

Hold Time (t_H): The minimum time that data must be held valid at the receiver input after the clock edge arrives at the receiver.

When a minimum time is listed for the source of a signal, it means that the source is guaranteed to drive that signal for at least that minimum time.

When a minimum time is listed for the receiver of a signal, it means that the source must drive that signal for at least that minimum time in order for the receiver to always receive it correctly.

When a maximum time is listed for the source of a signal, it means that the source is guaranteed to drive that signal no longer than that maximum time.

When a maximum time is listed for the receiver of a signal, it means that the source must drive that signal no longer than that maximum time in order for the receiver chip to work correctly.

Program Memory Characteristics

t_{LHLL}	ALE pulse width (ALE high to ALE low). This is the minimum amount of time that the processor will drive the ALE signal high.
t_{AVLL}	Address setup to ALE (address valid to ALE low). This is the minimum amount of time that the processor will provide valid address information at the Port 0 outputs prior to driving ALE to a low level. Compare this specification to the setup time for the ‘373 transparent latch (the minimum time the address must be held valid at the inputs of the ‘373 prior to its LE signal going low).
t_{LLAX}	Address hold after ALE (ALE low to address change). This is the minimum amount of time the processor will hold the address valid at the Port 0 outputs after ALE goes low during a program memory read cycle. Compare this specification to the hold time for the ‘373 transparent latch (the minimum time the address must be held valid at the inputs of the ‘373 after its LE signal goes low).
t_{LLIV}	ALE low to valid instruction in. This is the maximum amount of time external circuitry has to provide a valid instruction to the Port 0 inputs after ALE goes low.
t_{LLPL}	ALE to /PSEN (ALE low to /PSEN low). This is the minimum amount of time between when the processor drives ALE low to when it drives /PSEN low.
t_{PLPH}	/PSEN pulse width (/PSEN low to /PSEN high). This is the minimum amount of time that the processor will drive the /PSEN line low during a read cycle from external program memory space (either an instruction fetch or a read due to a MOVC).
t_{PLIV}	/PSEN to valid instruction in (/PSEN low to instruction valid). This is the maximum amount of time external circuitry has to provide a valid instruction to the Port 0 inputs after /PSEN goes low.
t_{PXIX}	Input instruction hold after /PSEN (/PSEN change to instruction change). This is the minimum amount of time that external circuitry (e.g. memory) must hold an instruction valid at the Port 0 inputs after /PSEN starts to transition from low to high.
t_{PXIZ}	Input instruction float after /PSEN (/PSEN change to instruction high impedance). This is the maximum amount of time external circuitry (e.g. memory) may drive a valid instruction to the Port 0 inputs after /PSEN starts to transition from low to high. If the external device continues driving the bus after this time, bus contention will occur between the memory device driving the bus and the processor trying to drive the next address on the bus. The memory device should float its outputs (go to a high impedance state) before the processor starts driving the bus.
t_{PXAV}	Address valid after /PSEN (/PSEN change to address valid). This is the minimum amount of time between when the processor starts driving /PSEN low to high and when the processor starts driving the next address on Port 0.
t_{AVIV}	Address to valid instruction in (address valid to instruction valid). This is the maximum amount of time external circuitry (e.g. memory) has to drive a valid instruction to the Port 0 inputs after the processor has driven a valid address on Port 0. The processor may sample its Port 0 inputs after this time has passed; therefore, external circuitry must meet this parameter in order to ensure the processor samples a valid instruction.
t_{AZPL}	Address float to /PSEN (address high impedance to /PSEN low). This is the minimum amount of time between when the processor stops driving an address on its Port 0 outputs to when the processor drives /PSEN low, thus enabling external circuitry (e.g. memory) to drive an instruction or data back to Port 0.

External Data Memory Characteristics

t_{RLRH}	/RD pulse width (/RD low to /RD high). This is the minimum amount of time that the processor will drive the /RD signal low during a data memory read cycle.
t_{WLWH}	/WR pulse width (/WR low to /WR high). This is the minimum amount of time that the processor will drive the /WR signal low during a data memory write cycle.
t_{LLAX2}	Address hold after ALE (ALE low to address change). This is the minimum amount of time the processor will hold the address valid at the Port 0 outputs after ALE goes low during a data memory read or write cycle. Compare this specification to the hold time for the '373 transparent latch (the minimum time the address must be held valid at the inputs of the '373 after its LE signal goes low).
t_{RLDV}	/RD to valid data in (/RD low to data valid). This is the maximum amount of time external circuitry has to provide valid data on to the Port 0 inputs after /RD goes low. The processor may sample its Port 0 inputs after this time has passed; therefore, external circuitry must meet this parameter in order to ensure the processor samples a valid data byte.
t_{RHDX}	Data hold after /RD (/RD high to data change). This is the minimum amount of time that external circuitry (e.g. memory) must hold data valid at the Port 0 inputs after /RD has transitioned from low to high.
t_{RHDZ}	Data float after /RD (/RD high to data high impedance). This is the maximum amount of time external circuitry (e.g. memory) may drive valid data to the Port 0 inputs after /RD has transitioned from low to high. If the external device continues driving the bus after this time, bus contention will occur between the memory device driving the bus and the processor trying to drive the next address on the bus. The external device should float its outputs (go to a high impedance state) before the processor starts driving the bus.
t_{LLDV}	ALE to valid data in (ALE low to data valid). This is the maximum amount of time external circuitry has to provide valid data to the Port 0 inputs after ALE goes low.
t_{AVDV}	Address to valid data in (Address valid to data valid). This is the maximum amount of time external circuitry (e.g. memory) has to drive valid data to the Port 0 inputs after the processor has driven a valid address on Port 0.
t_{LLWL}	ALE to /WR or /RD (ALE low to /WR low). During a data memory write cycle, after ALE is driven low, /WR will go low between the minimum and maximum times specified. During a data memory read cycle, after ALE is driven low, /RD will go low between the minimum and maximum times specified.
t_{AVWL}	Address valid to /WR or /RD (Address valid to /WR low). This is the minimum amount of time from when the processor provides valid address information at the Port 0 outputs prior to driving /WR to a low level during a data memory write cycle or /RD to a low level during a data memory read cycle.
t_{WHLH}	/WR or /RD high to ALE high (/WR high to ALE high). During a data memory write cycle, after /WR is driven high, ALE will go high between the minimum and maximum times specified. During a data memory read cycle, after /RD is driven high, ALE will go high between the minimum and maximum times specified.
t_{QVWX}	Data valid to /WR transition (Data valid to /WR change). This is the minimum amount of time that the processor will drive valid data information at the Port 0 outputs prior to starting to drive /WR low during a data memory write cycle. For external circuitry which latches the data relative to the falling edge of /WR, this value should be compared to the external circuitry's setup time.
t_{QVWH}	Data setup before /WR (Data valid to /WR high). This is the minimum amount of time that the processor will drive valid data information at the Port 0 outputs prior to starting to drive /WR high during a data memory write cycle. For external circuitry which latches the data relative to the rising edge of /WR, this value should be compared to the external circuitry's setup time.
t_{WHQX}	Data hold after /WR (/WR high to data change). This is the minimum amount of time that the processor will drive valid data information at the Port 0 outputs after driving /WR high during a data memory write cycle. For external circuitry which latches the data relative to the rising edge of /WR, this value should be compared to the external circuitry's hold time.
t_{RLAZ}	Address float after /RD (/RD low to address high impedance). This is the maximum amount of time that the processor will continue to drive address information on Port 0 after /RD has been driven to a low level during a data memory read cycle.