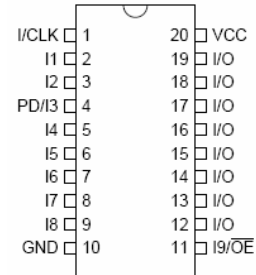


# Introduction to Atmel ATF16V8C and WinCUPL

## ATF16V8C SPLD Features

- Industry-standard Architecture
  - Emulates Many 20-pin PALs®
  - Low-cost Easy-to-use Software Tools
- High-speed Electrically-erasable Programmable Logic Devices
  - 5 ns Maximum Pin-to-pin Delay
- Low-power - 100  $\mu$ A Pin-controlled Power-down Mode Option
- CMOS and TTL Compatible Inputs and Outputs
  - I/O Pin Keeper Circuits
- Advanced Flash Technology
  - Reprogrammable
  - 100% Tested
- High-reliability CMOS Process
  - 20 Year Data Retention
  - 100 Erase/Write Cycles
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Commercial and Industrial Temperature Ranges
- Dual-in-line and Surface Mount Packages in Standard Pinouts
- PCI Compliant



## Designing with the CUPL Language

Table 2-1. Using Number Bases

Number	Base	Decimal Value
'b'0	Binary	0
'B'1101	Binary	13
'O'663	Octal	435
'D'92	Decimal	92
Number	Base	Decimal Value
'h'BA	Hexadecimal	186
'O'[300..477]	Octal (range)	192..314
'H'7FXX	Hexadecimal (range)	32512..32767

Table 2-2. Logical Operators

Operator	Examples	Description	Precedence
!	!A	NOT	1
&	A & B	AND	2
#	A # B	OR	3
\$	A \$ B	XOR	4

See the Atmel – WinCUPL User's Manual for more information.

# General WinCUPL File Structure (.PLD)

```
Name      Gates08;
Partno    ESD001;
Revision  01;
Date      1/22/2008;
Designer  I.M. Good;
Company   University of Colorado;
Location  None;
Assembly  None;
Device    gl6v8a;
```

Tip: Header information for WinCUPL source file (.PLD) and WinSim input file (.SI) must match.

```
/*
 *
 * General File Comments
 *
 */

/*
 * Inputs:  define inputs in this section
 */

/*
 * Outputs: define outputs as active HI levels in this section
 */

/*
 * Logic:   logic equations in this section
 */
```

## WinCUPL Syntax Example

```
/*
 * Inputs:  define inputs to build simple gates from
 */

Pin 1 = a;
Pin 2 = b;

/*
 * Outputs: define outputs as active HI levels
 */

Pin 12 = inva;
Pin 13 = invb;
Pin 14 = and;
Pin 15 = nand;
Pin 16 = or;
Pin 17 = nor;
Pin 18 = xor;
Pin 19 = xnor;

/*
 * Logic:  examples of simple gates expressed in CUPL
 */

inva = !a;          /* inverters */
invb = !b;
and  = a & b;       /* and gate */
nand = !(a & b);    /* nand gate */
or   = a # b;       /* or gate */
nor  = !(a # b);    /* nor gate */
xor  = a $ b;       /* exclusive or gate */
xnor = !(a $ b);    /* exclusive nor gate */
```

Tip: Use circuit signal names like A15, PSEN, RD, etc.

Tip: Use circuit signal names like CSROM, READ, etc.

# General WinSim File Structure (.SI)

```
Name      Gates08;
Partno    ESD001;
Revision  01;
Date      1/22/2008;
Designer  I.M. Good;
Company   University of Colorado;
Location  None;
Assembly  None;
Device    gl6v8a;
```

Tip: Header information for WinCUPL source file (.PLD) and WinSim input file (.SI) must match.

```

/*****
/*
/*      General File Comments
/*
/*
/*****

/*
* Order:  define order, polarity, and output spacing of stimulus and response values
*/

/*
* Vectors:  define stimulus and response values, with header
* and intermediate messages for the simulator listing.
*
* Note: Don't Care state (X) on inputs is reflected in outputs where appropriate.
*/
```

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5

## WinSim Syntax Example

```

/*
* Order:  define order, polarity, and output spacing of stimulus and response values
*/

ORDER: a, %2, b, %4, inva, %3, invb, %5, and, %8, nand, %7, or, %8, nor, %7, xor, %8, xnor;

/*
* Vectors:  define stimulus and response values, with header
* and intermediate messages for the simulator listing.
*
* Note: Don't Care state (X) on inputs is reflected in outputs where appropriate.
*/

VECTORS:
$MSG "          Simple Gates Simulation";
$MSG "          inverters and      nand      or      nor      xor      xnor";
$MSG "          a b      !a !b      a & b      !(a & b)      a # b      !(a # b)      a $ b      !(a $ b)";
$MSG "          - -      - -      - - - - -      - - - - -      - - - - -      - - - - -      - - - - -";
00HLLHLLH
01HLLHLLH
10LHLLHLL
11LLHLLH
1XLXXXHLX
X1LXXXHLX
0XHLHXXXX
X0XHLHXXXX
XXXXXXXXX
```

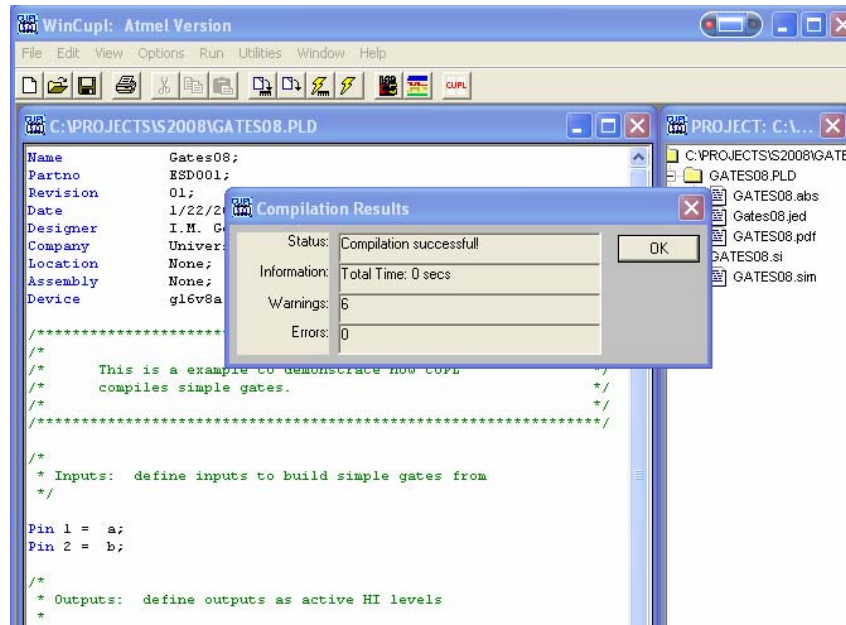
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6

# WinCUPL Warnings

(due to header mismatch between .PLD and .SI files)



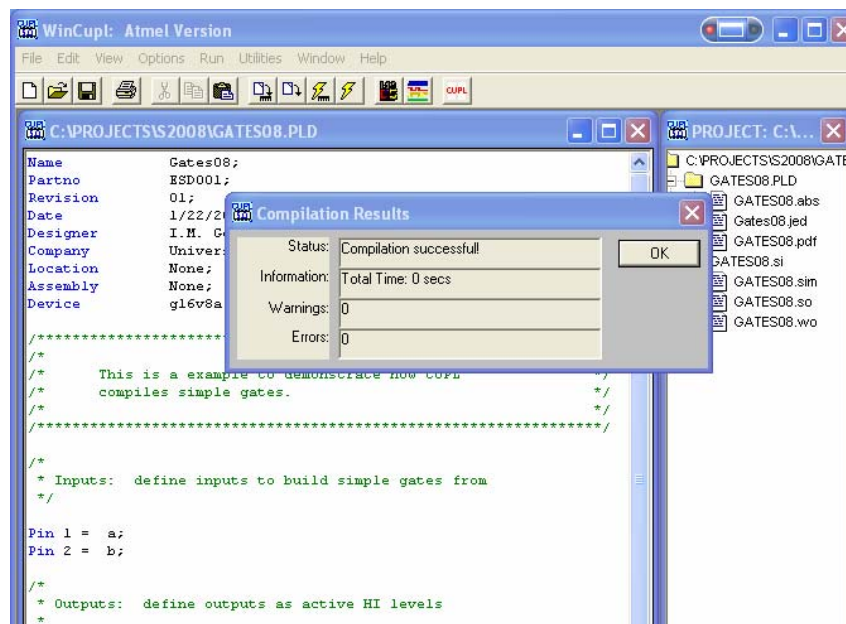
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7

# WinCUPL Success

(after making headers match)

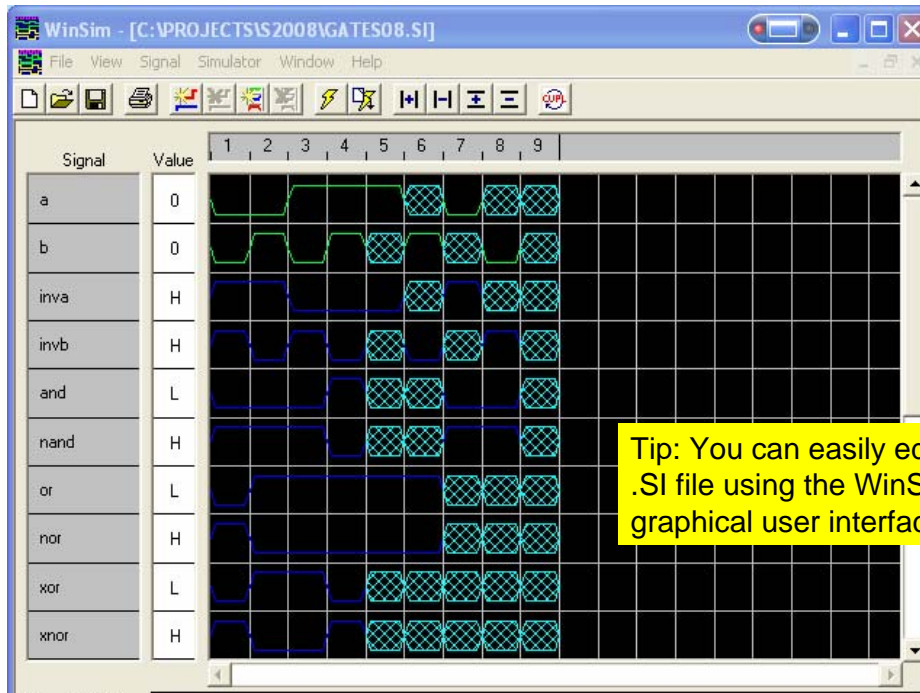


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8

# WinSim Screen After Simulation

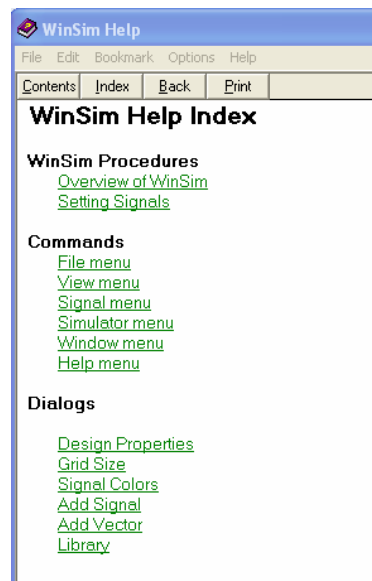
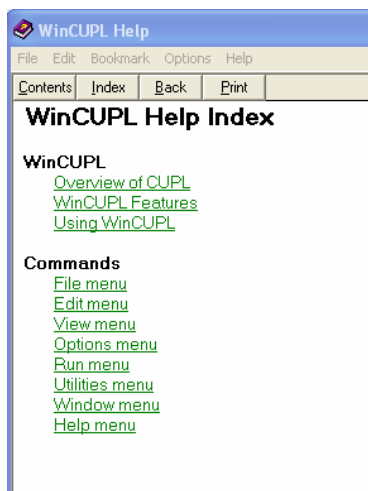


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9

# WinCUPL/WinSim Integrated Help



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10

# Notes

- ❑ If you change the header info in the .PLD file, you also need to change the header information in the .SI file. If the headers don't match, you'll get errors.
- ❑ Look in the .SO file to see the errors encountered during simulation in WinSim. They don't appear on the screen or in the simulator error window.
- ❑ **Students have reported that the negative polarity declaration on output pins does not work. The code compiles without error, but the actual SPLD doesn't seem to work. Be forewarned! I recommend you declare active HI outputs and avoid using negative polarity.**
- ❑ If you use FIELD to define a bus segment that doesn't begin at bit 0, and if you want to compare that bus segment with a constant value, you need to pad the constant with don't cares, so that the FIELD bits are being compared with the same bits in the constant. A 32-bit value is used by the WinCUPL to hold FIELD values.

```
FIELD ADDR = [A15..A12]; /* Define ADDR as a field of four inputs (A15, A14, A13, A12) */

/* Compare with least significant xxxx nybbles of 32-bit value */
/* Two syntax options are shown below - choose one */

CSROM = !(ADDR:0xxx # ADDR:1xxx # ADDR:2xxx # ADDR:3xxx # ADDR:4xxx # ADDR:5xxx);

CSROM = !(ADDR:[0xxx..5xxx]); /* CSROM low for addresses 0000h-5FFFh */
```

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11

# Notes

- ❑ See the examples in the WinCUPL\Examples directory.
- ❑ Read the documents in the WinCUPL Help menu, including the programmer's reference guide and the Atmel Info link (errata, tutorial, etc.)
- ❑ You can use the GUI of the WinSim tool to create (and modify) your .SI file. However, you may need to hand edit that file if you want to change things like the header information, etc.
- ❑ Read the CUPL Programmer's Reference Guide, which is available through the WinCUPL Help menu. There is a lot of information there.
- ❑ Read the Atmel - WinCUPL User's Manual, which is available through the Atmel WinCUPL web page and on the course home page.
- ❑ Search Google for ".pld CUPL"
  - <http://ee.usc.edu/library/ee459/>
  - [http://ee.usc.edu/library/ee459/documents/PALCE22V10\\_Notes.pdf](http://ee.usc.edu/library/ee459/documents/PALCE22V10_Notes.pdf)
  - Pretty good CUPL tutorial
  - <http://www.rexfisher.com/Downloads/CUPL%20Tutorial.htm>
- ❑ Other resources are available on the web

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12