

5000-level Independent Study Opportunity - Embedded Systems PCB Design, USB, FPGAs, Signal Integrity

Prerequisites

- ECEN 4013/5013/4613/5613 with a grade of an A or A-; good overall GPA
- Ability to work independently and in small groups; self-motivated and ambitious
- Ability to meet on at least 8 Saturdays for group meetings with instructor
- Instructor consent (application form required)

Objectives

- Design 2-layer or 4-layer PCB with some or all of the following features (TBD):
 - Cypress EZ-USB FX or EZ-USB FX2 processor (core at 48 MHz), USB connector
 - FPGA, CPLD, GAL
 - Compact Flash Type II? connector
 - Flash chip interface
 - SRAM interface
 - I/O Expander (I2C, 400 kHz)
 - EEPROM (I2C, 400 kHz)
 - RS-232 connectors, RS-232/RS-485 line driver support, jumpers to select path
 - LCD interface, PS/2 connector(s), video connector?
 - Push-button and DIP switches, LED driver circuits, 7-segment displays
 - 4+ channel DAC, 4+ channel ADC
 - FET drivers for stepper motor, isolated power
 - ATA/ATAPI (IDE) interface
 - Linear regulators (5V, 3.3V, 2.5V,...), load option for bus-powered/self-powered device
 - Prototype area (0.1"x0.1" matrix of holes)
 - Multi-output clock synthesizer and various routing and termination techniques
 - Supervisory circuit
 - Network I/F (chip and connector)? PCI I/F?
 - Cypress PSoC footprint??
 - Debugging support (test points, ground/power pins, probe points, logic analyzer, clock shmoo, voltage shmoo, etc.)
 - Load options (zero ohm connections, pull-ups, pull-downs)
 - Decoupling capacitors (through hole, surface mount), good power/ground routing
 - Breakouts for various surface mount packages for prototyping/adapters
 - (other feature ideas determined by looking at other commercial embedded systems)
- Develop PCA
- Test stability of power circuits, measure noise on power rails, optimize decoupling
- Test signal integrity, explore termination techniques
- Learn development environment (Cypress, Keil)
- Exercise I2C bus and DMA
- Develop reading list and materials for future course offering
- Analyze USB signals, protocol (with scope and CATC USB Chief analyzer/software)

Possible Projects

- Implement USB peripheral
- Write user interface/driver for Windows/Linux? Linux development environment?
- Implement Verilog code in FPGA, possibly implement custom processor core
- Get PAULMON2 and SDCC running with this architecture
- Compact flash card reader (FAT file system support), upload files/pictures
- Media reader/Removable drive (Compact Flash and/or other formats)
- Multitasking kernel

Logistics

- No required text books
- Required: Cypress EZ-USB FX technical reference manual and data sheet (PDF)
- Several recommended books, some available from instructor for temporary use.
Examples: USB Design By Example; USB Complete; Universal Serial Bus System Architecture (2nd Edition); High-Speed Digital Design; Programming the Microsoft Windows Driver Model (2nd Edition); Verilog HDL Synthesis - A Practical Primer
- Various application notes and data sheets
- No fixed, organized lectures. Instructor and students will meet periodically to discuss objectives, assigned reading, progress, next steps. Demos will take place on-campus.
- No dedicated TA: Students are expected to help each other - this is a course requirement.
- Much of the work can be done off campus, if desired by the student.
- Schematics and PCB layout to be done with Orcad tools (Capture CIS and Layout).
- Students should expect to spend at least \$100 each for lab materials (PCB, parts).
- Electronic copies of all design files (schematics/layout/BOM/code/etc.) to be left with the instructor for use in future classes. Future designs may leverage these designs.
- One populated and working board must be given to the instructor by each team for use in future semesters. This board should be included as part of the final project report.
- Some funds might be available from the instructor to help in covering PCB cost. TBD.

Schedule (tentative)

- Jan: Course objectives, reading, use existing USB board and development environment, brainstorm new board features and PCB layout ideas. Finish schematics.
- Feb: Schematic design review. PCB layout. Layout design review and schematic/BOM freeze. Order boards and components. Prepare test plan and bring-up plan for PCA. Analyze USB protocol traces with CATC software. Continue using development environment on existing USB board. Develop bring-up code modules. Milestone 1.
- Mar: Assemble PCA, get USB I/F working with development environment, RS-232, processor core running at 48MHz. I2C at 400 kHz (I/O expanders, EEPROM (boot loader), data converters?). Interrupts. Performance challenge (throughput). Milestone 2.
- Apr: FPGA and Verilog. Final project.
- May: Demo and report (including scope traces, etc.), update web site with URLs/pictures.

Grading (tentative)

- 20% Participation and contributions to the class, attitude, initiative and self-motivation
- 20% Milestone 1
- 20% Milestone 2
- 40% Final Project (hardware, software, documentation, presentation)

Possible layout:

