Application Of One-Cycle Control To Three-Phase High Quality Resonant Rectifier

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Abstract - A voltage feedforward control technique based on one-cycle control concept is introduced. This technique is applied to a single switch three-phase high quality resonant rectifier. The controller does not eliminate the line current harmonics totally, however it does produce a well-regulated dc output voltage. The controller causes the adjacent harmonics in the line current to be of equal magnitude. The overall effect on the input line current is lower harmonic distortion. Also, introduced in this paper is a small-signal modeling technique suitable for three-phase ac–dc PWM single switch rectifiers. Theoretical analysis is supported with simulation results.

I. INTRODUCTION

Recently, many 3φ high power factor rectifiers employing a single switch topology have been introduced [1-8]. The proposed rectifiers perform the function of high power factor/low harmonic rectification naturally, without need to sense the input line current in order to obtain a high quality line current waveform. In fact, most of the proposed rectifiers in [1-8] have been simulated and/or constructed running open-loop. However, closed-loop operation becomes a requirement when it is desired to regulate the system at a nominal operating point. Deviations result from disturbances in the source voltage and/or load current. The objective of this paper is to explore some control schemes and modeling techniques for the proposed rectifiers.

Section II discusses the relation between harmonic currents and harmonic power in a typical 3φ rectifier system. Such analysis is important in a regulated 3φ ac–dc rectifier system. The result that harmonic power can flow in the ac section of the rectifier even though the instantaneous power is constant is obtained and supported with simulation results. This result is obtained based on both Fourier series and symmetrical components analysis.

Section III introduces a voltage feedforward control technique based on one-cycle control concept. The one-cycle control method was introduced in [9] to control dc–dc switching converters. Moreover, this technique has been further explored in [10] and applied to 3φ ac–dc single switch conventional PWM buck-type rectifier. The one-cycle control has the same advantages as the conventional voltage feedback control or current mode control. It has additional advantages over the conventional control techniques. These advantages include:

- Well regulated dc output voltage.
- Simple circuit implementation.
- Reduction of the line current total harmonic distortion.
- Better dynamic response and stable control loop.
- Control loop is insensitive to noise.

The principle of one-cycle control method is extended in this paper and it is applied to 3φ ac–dc single switch resonant rectifiers presented in [2, 3].

Finally, Section IV presents step-by-step modeling procedure in order to model 3φ ac–dc PWM single switch rectifiers. The modeling technique is suitable for both rectifiers having boost-type (inductive) input or buck-type (capacitive) input introduced in [2].

II. HARMONIC CURRENT AND POWER IN 3φ RECTIFIER SYSTEM

Any periodic waveform can be decomposed into a Fourier series consisting of a dc value and higher order harmonics, that is:

\[
i(t) = I_{dc} + \sum_{n=1}^{\infty} I_n \cos(n\omega_0 t + \phi_n)
\]

which can be expressed in terms of phasors as,

\[
i(t) = I_{dc} + \text{Re} \left[ \sum_{n=1}^{\infty} I_n e^{j(n\omega_0 t + \phi_n)} \right]
\]

where Re[x] is the real part of x. Next, we determine the sequence of the harmonic line currents in a 3φ rectifier system excited by three pure sinusoidal voltages with 120° phase shift. That is,

\[
v_{an}(t) = \text{Re}[V_m e^{j(\omega t + \pi/6)}]
\]

\[
v_{bn}(t) = \text{Re}[V_m e^{j(\omega t + \pi/2)}]
\]

\[
v_{cn}(t) = \text{Re}[V_m e^{j(\omega t + 5\pi/6)}]
\]

(3)
Where $V_m$ is the peak input line-neutral voltage and the operator $a = e^{j120^\circ}$. Thus, we may assume the system under consideration is symmetrical and of positive phase sequence. The three line currents will be then identical except for $\pm 120^\circ$ phase shift. Then, from (2), the three line currents can be expressed as,

\[
i_a(t) = \text{Re} \left[ \sum_{n=1}^{\infty} I_n e^{j(n \omega t + \theta_n)} \right]
\]

\[
i_b(t) = \text{Re} \left[ \sum_{n=1}^{\infty} j n \left( \omega t - 120^\circ \right) e^{j(n \omega t + \theta_n)} \right]
\]

\[
i_c(t) = \text{Re} \left[ \sum_{n=1}^{\infty} j n \left( \omega t + 120^\circ \right) e^{j(n \omega t + \	heta_n)} \right]
\]

Where $I_n$ is set to zero due to the waveform symmetry. Expanding (4), one can deduce the following:

1. The fundamental component and harmonics of order of $3n+1$ where $n$ is an integer, are in positive phase sequence coordinate.
2. Harmonics of order $3n-1$ are in negative phase sequence coordinate.
3. Harmonics of order $3n$ (i.e. triple-$n$ harmonics) are in zero phase sequence coordinate.

Furthermore, even harmonics cannot flow in the line currents, since the line-line voltages are odd functions and contain no even harmonics. Similarly, triple-$n$ harmonics do not exist in the line-line voltages, hence, they cannot be applied to the diode rectifier bridge. As a result, no triple-$n$ harmonics can flow in the line currents. This will reduce (4) to:

\[
i_a(t) = \text{Re} \left[ \sum_{n=1,5,7,...}^{\infty} I_n e^{j(n \omega t + \theta_n)} \right]
\]

\[
i_b(t) = \text{Re} \left[ \sum_{n=1,5,7,...}^{\infty} j n \left( \omega t - 120^\circ \right) e^{j(n \omega t + \theta_n)} \right]
\]

\[
i_c(t) = \text{Re} \left[ \sum_{n=1,5,7,...}^{\infty} j n \left( \omega t + 120^\circ \right) e^{j(n \omega t + \theta_n)} \right]
\]

The total instantaneous power at the input port of $3\phi$ system with balanced input voltage is given by:

\[
P_a = P_x + P_y + P_z,
\]

where

\[
P_x = \frac{1}{2} V_m I_1 \cos(\theta_1)
\]

\[
P_y = \frac{1}{2} V_m I_{n+1} \cos \left( n \omega t + \theta_{n+1} \right) - I_{n-1} \cos \left( n \omega t + \theta_{n-1} \right)
\]

where $n=6m$ and $m$ is an integer. Table I shows that the harmonic power of order 2, 8, 14, ... are in the negative phase sequence, while the harmonic power of order 4, 10, 16, ... are in the positive phase sequence. These harmonic powers do not contribute to the average power since their sum reduces to zero. Only harmonic power of order $6n$ where $n$ is an integer (including $n=0$), which are in the zero phase sequence, contribute to the overall power. Thus, (6) can be expressed by the following general formula,

\[
P_{dc} = P_x + P_y
\]

where

\[
P_{dc} = 3 P_0 + \frac{3}{2} V_m I_1 \cos(\theta_1)
\]

\[
P_y = \frac{3}{2} V_m \sum_{n=1}^{\infty} I_{6n+1} \cos \left( 6n \omega t + \theta_{6n+1} \right)
\]

\[+ I_{6n-1} \cos \left( 6n \omega t + \theta_{6n-1} \right)
\]

The total harmonic power decomposition for a three-phase rectifier system is given in Table I.

<table>
<thead>
<tr>
<th>Harmonic Power Decomposition for a Three-Phase Rectifier System</th>
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<tbody>
<tr>
<td>$P_a$</td>
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<tr>
<td>$P_0$</td>
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<td>$P_x$</td>
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<td>$P_y$</td>
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<td>$P_z$</td>
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<td>$P_{dc}$</td>
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It can be seen from (8), that harmonic power, $P_h$, is present at the input port of the 3\(\phi\) system due to existence of harmonic line currents. Thus, harmonic power can flow in the ac side of the rectifier even though the instantaneous power is constant. When designing a regulated 3\(\phi\) ac-dc rectifier, equation (8) plays an important role in deciding whether the controller should remove the higher order harmonic components from the dc output voltage or not. This argument will be explored in more detail in the next section.

III. THREE-PHASE RESONANT SWITCH RECTIFIERS WITH ONE-CYCLE CONTROL

Recently, a new class of 3\(\phi\) ac-dc resonant switch rectifiers featuring zero-current-switching (ZCS) and zero-voltage-switching (ZVS) were introduced in [2, 3] respectively. Moreover, it was shown in [2, 3], with a single controllable switch operating at either ZCS or ZVS, a high quality input current can be obtained simply in open-loop operation. This is because the new rectifiers present an approximate three-phase resistive load to the ac source. The total harmonic distortion in the ac line current for these rectifiers is in the neighborhood of 12% depending on the operating point. Moreover, most of this distortion results from the fifth harmonic component while the remaining harmonic components are almost negligible.

Introduced here is a technique suitable for regulation of the output voltage in the 3\(\phi\) ZCS resonant switch rectifiers presented in [2]. At the same time, this method also reduces the fifth harmonic component to a lower value, while it boosts the seventh harmonic component to be equal to the fifth harmonic component. As a result, the total harmonic distortion in the line current is reduced.

Fig. 1 shows a 3\(\phi\) ZCS buck rectifier with the proposed feedback controller. The control method is known as one-cycle control introduced in [9] to control dc-dc switching converters.

The control concept is based on controlling the switch duty cycle in real time such that during each cycle the average value of the switched waveform at the output diode of the switch rectifier is equal to the control reference. The output voltage of the rectifier of Fig. 1, is the average value of the tank capacitor voltage $V_{ca}$ which is the area under each tank capacitor voltage $V_{ca}$ pulse divided by the switching period,

$$V_{ca} = \frac{1}{T_s} \int_0^{T_s} V_{ca} \, dt \tag{9}$$

This voltage is subtracted from a reference voltage $V_{ref}$ and then fed back to a real-time integrator. If the control reference is constant, then the average value of $V_{ca}$ is constant, hence the output voltage is also constant. When the integrator output waveform reaches zero (i.e. when the average tank capacitor voltage reaches the reference voltage $V_{ref}$) the power switch is turned on and the integrator is reset to zero to prepare to the next cycle. The comparator output is fed to a circuit to produce gating signal for the SCR power switch.

The tank capacitor voltage waveform may be different during each cycle, however, as long as its average value is equal to the reference value, instantaneous control of the tank capacitor voltage is achieved. Fig. 2, shows various controller waveforms at point of common interest over one switching period.

What is the effect of the controller on the line current harmonics? As mentioned earlier, the output voltage is constant and contains no 360 Hz component. Thus, the output voltage is a pure dc leading to a dc output power. Moreover, for a lossless 3\(\phi\) network, the total instantaneous input power which is given by (8) must equal the output power. Thus, the input harmonic power $P_h$ given in (8) must equal to zero. Investigating (8) shows that one possibility that $P_h$ is zero is when the adjacent harmonic current components of order $0 \leq n \leq 1$ where $n$ is an integer are equal in magnitude (i.e. $I_n = I_{n+6}$, $I_{n+12}$, $I_{n+18}$, etc.). Fig. 3(a). This conclusion is confirmed by simulation results. Fig. 3(b), shows the effect of implementing one-cycle-control scheme on the power propagation in a 3\(\phi\) rectifier system. As can be seen from Fig. 3(b), only the fundamental power passes through to the output load, while the harmonics powers circulate through the ac-side of the rectifier.

The circuit of Fig. 1 has been simulated for a power level of 23.6 kW with the following circuit parameters: $V_{ref}=440$ V, $C=1.25$ mF, $L=14.6$ mH, $V_{ref}=370$ V. The load was changed from 5.8 \(\Omega\) to 4.8 \(\Omega\) after 20 m sec. The simulated input line current for phase a is shown in Fig. 4 with a total harmonic distortion in the line current approximately 10% with unity displacement. Both the fifth and seventh harmonic components were equal to 7.1%. Fig. 5, shows the simulated output voltage which follows the reference voltage $V_{ref}$. The previous results shows that the one-cycle controller does not eliminate line current harmonics totally, but it will produce a well regulated dc output voltage.

The same control method can be used for the 3\(\phi\) ZVS rectifiers presented in [3]. It can be also implemented for 3\(\phi\) multi-resonant rectifier class introduced in [6, 8]. For example, consider applying this control technique to the 3\(\phi\) ZVS boost rectifier of Fig. 6, for constant load current applications. The controller should sense the tank inductor current $i_c$, instead of sensing the tank capacitor voltage since the output load current is determined by the average value of $i_c$.

The average of the tank inductor current $i_c$, is subtracted from a dc reference current value $I_{dc}$ and then fed back to a real-time integrator. If the control reference current is constant, then the average value of $i_c$ is constant, hence the output load current is also constant. The integrator output is then compared to a zero value to produce the required gating signal.

![Fig. 1 3\(\phi\) ZCS buck rectifier with feedback controller.](image-url)
IV. MODELING 3φ DCM-PWM RECTIFIERS

Even though the proposed rectifiers in [1-8] perform the function of high quality rectification naturally, it may become necessary in some applications to obtain a better system response by use of feedback control. When feedback control is used, then it is necessary to have at least a small-signal model, in order to correctly design the controller. Many have addressed modeling techniques for dc-dc converters operating in either continuous conduction mode (CCM), or in discontinuous conduction mode (DCM) [11, 12], whereas few authors extend these techniques to model single phase ac-dc rectifiers [13-17].

Three different control schemes are introduced and applied to the 3φ ac-dc DCM boost rectifier system in [18]. However, the objective of this section is to derive a small signal averaged model for the 3φ ac-dc DCM boost rectifier which can be easily extended to the other rectifiers falling in this class. Such an analysis was not addressed before.
Introduce in this section is a technique suitable for modeling the rectifiers of [2], i.e., 3φ ac-dc PWM high power factor (HPF) rectifiers whose input line inductors or input line-line capacitors are operating in DCM, [2]. An analysis example of one of the rectifiers whose input line inductors are operating in DCM is considered here, whereas the same technique can be implemented for the rectifiers with capacitive input operating in DCM.

The 3φ ac-dc PWM boost HPF rectifier, Fig. 7, is considered as an example here. The modeling procedure for single phase ac-dc boost HPF rectifier operating in DCM is given in [17]. An extension to 3φ case is considered next.

A. Modeling 3φ Ac-DC Boost HPF-PWM Rectifier

Fig. 7. shows a 3φ HPP boost rectifier. The three supply phase voltages are given by

\[ v_a = V_m \sin(\omega t) \]
\[ v_b = V_m \sin(\omega t - 120^\circ) \]
\[ v_c = V_m \sin(\omega t + 120^\circ) \]  \( \text{(10)} \)

are assumed to be balanced and symmetric with a peak voltage of \( V_m \). The frequency of the supply voltage (50Hz or 60Hz) is assumed to be much lower than the switching frequency of the power switch \( Q \). Owing to the circuit symmetry, it is sufficient to consider a 30° interval. There are six different intervals during each half-cycle, each of length 30°, while there are four subintervals during each switching period. The three line inductors \( L \) operate in the discontinuous conduction mode (DCM), while the output filter capacitor, \( C_p \), is chosen to operate in continuous conduction mode (CCM). The circuit functions as a high power factor/low harmonic rectifier based on the concept that the peak of the input line currents are proportional to the input phase voltage. Thus, the low frequency components of the input line current follow approximately the input phase voltage. The circuit equations over one switching period are given next. The first 30° interval where \( t_0 < t_\leq t_1 \) is considered here.

Subinterval 1, \( t_0 < t < t_1 \). \( Q \) is ON and \( D \) is OFF

In this interval the three line currents are given by

\[ i_\phi(t-t_0) = \frac{v_0}{L} (t-t_0) \quad \phi = a, b \text{ and } c \]  \( \text{(11)} \)

Thus, the three line currents in each phase increase linearly from zero, at a rate proportional to their respective phase voltages. The peak values of these currents occur at the end of this subinterval, and are given by

\[ i_{t,\phi} = \frac{D}{2L} T_s v_\phi(t_k) \quad \phi = a, b \text{ and } c \]  \( \text{(12)} \)

where

\[ t_k = (k - 1 + D) T_s \]

and \( k \) is an integer. The variable \( D \) is the switch duty cycle and \( T_s \) is the switching period.

Subinterval 2. \( t_1 < t < t_2 \). \( Q \) is OFF and \( D_1, D_3, D_5 \) and \( D \) are ON

![Fig. 7 3φ ac-dc boost high power factor rectifier.](image)

The second subinterval starts when the switch is turned off and the output diode \( D \) conducts along with \( D_1, D_3 \) and \( D_5 \). During this subinterval, the inductor currents discharge towards the ground level, with the smallest current (\( i_a \) for \( D_1 D_3 D_5 \) interval) reaching zero first. The rate of discharge is proportional to the output voltage \( v_c \). The circuit equations are given by

\[ v_{L_a} = v_a - \frac{V_{CP}}{3} \]
\[ v_{L_b} = v_b + \frac{2V_{CP}}{3} \]
\[ v_{L_c} = v_c - \frac{V_{CP}}{3} \]  \( \text{(13)} \)

Subinterval 3. \( t_2 < t \leq t_3 \). \( Q \) is OFF and \( D_3, D_5 \) and \( D \) are ON

During this subinterval, the remaining two currents (\( i_a \) and \( i_c \) for the \( D_1 D_3 D_5 \) interval) discharge to zero. The circuit equations are given by

\[ v_{L_a} = 0 \]
\[ v_{L_c} = -v_{L_b} = \frac{1}{2} (v_a - v_b - v_{CP}) \]  \( \text{(14)} \)

All three input line currents remain at zero during the fourth subinterval. Fig. 8, shows the circuit waveforms over one switching period. The remaining 60° intervals can be analyzed following the same procedure.

From (12), one can define piecewise constant current for \( i_a, i_b, \) and \( i_c \) as

\[ i_{1a} = \frac{1}{2} i_{1ka} = \frac{D}{2L} T_s v_a(t_k) \]
\[ i_{1b} = \frac{1}{2} i_{1kb} = \frac{D}{2L} T_s v_b(t_k) \]
\[ i_{1c} = \frac{1}{2} i_{1kc} = \frac{D}{2L} T_s v_c(t_k) \]  \( \text{(15)} \)

The length of \( d_{ik} \) and \( m_{ik} \) shown in Fig. 8, can be determined by applying volt-sec balance to both \( v_{L_a} \) and \( v_{L_b} \), thus one obtain

\[ d_{ik} = \frac{D}{v_a(t_k)} \frac{v_a(t_k)}{3} - v_a(t_k) \]
\[ d_{ik} + m_{ik} = \frac{D}{v_a(t_k)} \frac{v_a(t_k) - v_b(t_k)}{v_b(t_k) - v_c(t_k) + v_{CP}} \]  \( \text{(16)} \)
The average equation for the output capacitor current $i_{CP}$ over $f_1/6$, where $f_1$ is the line frequency is

$$i_{CP} = C_F \frac{dV_{CP}}{dt} = i_d - i_0 \quad (17)$$

where

$$I_0 = \frac{V_{CP}}{R}$$

and $i_d$ is the average output diode D current for $1/(6f_1)$ of ac source period. This current is given for $0 \leq \omega t \leq \pi/3$ interval by

$$i_d = 6 f_1 \sum_{k=1}^{n} (d_{ik} + m_{ik}) T_k \left(i_{1kb} - i_{1kb} \right) \quad n = \frac{T_k}{6 T_1} \quad (18)$$

Substitution of (15) and (16) into (18) and evaluate (17), one obtains

$$\frac{dV_{CP}}{dt} = \frac{-V_{CP}}{RC_F} + \frac{3 \omega T_c^2}{2 \pi L C_F} \sum_{k=1}^{n} D \left(v_b(t_k) - v_c(t_k)\right) \quad (19)$$

where $D = D_o + \hat{d}$ and $v_{CP} = v_o + \hat{v}_{CP}$, then perturb and linearize (19), one obtains a DC term and an AC term. These terms are given

**DC term:**

$$\frac{V_o}{RC_F} = K_1 \sum_{k=1}^{n} \frac{D_o}{v_b(t_k) - v_c(t_k)} + V_o \quad (20)$$

**AC term:**

$$\frac{dV_{CP}}{dt} = \frac{-i_{CP} + 2D_o K_1 \sum_{k=1}^{n} \frac{v_b(t_k) - v_c(t_k) + V_o}{v_b(t_k) - v_c(t_k) + V_o}}{2 \pi L C_F} \quad (21)$$

where

$$K_1 = \frac{3 \omega T_c^2}{2 \pi L C_F}$$

Further simplification is possible for both (20) and (21). Since $n >> 1$, then if one defines

$$A = \sum_{k=1}^{n} \frac{(v_c(t_k) - v_b(t_k))}{(v_b(t_k) - v_c(t_k) + V_o)^2} v_b(t_k) \quad (\omega T_c)$$

and

$$B = \sum_{k=1}^{n} \frac{(v_b(t_k) - v_c(t_k))}{(v_b(t_k) - v_c(t_k) + V_o)^2} v_b(t_k) \quad (\omega T_c)$$

Then (20) and (21) can be approximated by

$$\frac{V_o}{R} = \frac{3 T_k D_o}{2 \pi L} B \quad (22)$$

$$\frac{dV_{CP}}{dt} = \frac{-i_{CP} + 3 T_k D_o \frac{A}{2 \pi L C_F} V_{CP} + 3 T_k D_o B}{2 \pi L C_F} \quad (25)$$

respectively. The coefficients A and B are evaluated in closed form, and they are given by

$$A = \frac{-\pi}{6} + \frac{3 M^2}{4 (3-M^2)^2} \left[ \frac{M - \sqrt{3}}{M - \sqrt{3}} \right]$$

$$+ \frac{1}{2 \sqrt{3}} \left[ \frac{M - \sqrt{3}}{M - \sqrt{3}} + \ln \left( \frac{M - \sqrt{3}}{M - \sqrt{3}} \right) \right]$$

$$+ \frac{1}{\sqrt{M^2 - 3}} \left[ 2 M + \frac{M^3}{3 - M^2} \right] \tan^{-1} \left( \frac{M + \sqrt{3}}{3 (M - \sqrt{3})} \right) \quad (26)$$
and

\[
\frac{B}{V_m} = -1 \cdot \frac{M}{2} \left[ \frac{\pi}{3 + \sqrt{3}} \ln \left( \frac{M - \sqrt{3}}{2} \right) + \frac{2M}{\sqrt{M^2 - 3}} \tan^{-1} \left( \frac{M + \sqrt{3}}{3(M - \sqrt{3})} \right) \right]
\]

where \( M = V_d / V_m \). Application of Laplace transform to (25), one can easily obtain the control to output transfer function. This transfer function is given by

\[
\frac{\delta C_e(s)}{d(s)} = \frac{K_3}{K_2 + s}
\]

where

\[
K_2 = \frac{1}{C_F} \left( \frac{1}{R} + \frac{1}{r_1} \right) \quad \text{and} \quad K_3 = \frac{K_0}{C_F}
\]

and

\[
r_1 = -\frac{BR}{AV_m} \quad \text{and} \quad K_0 = \frac{2V_0}{D_0 R}
\]

Thus the rectifier of Fig. 7, has a single pole at frequency \( K_2 / 2\pi \) [Hz]. Hence, the feedback loop can be designed easily.

Fig. 9, shows the generalized \( Y \)-parameter model for the dc port of the rectifier. The term \( v_c \) is the control input voltage to the pulse-width modulator. For the rectifier of Fig. 7,

\[
y_{22}(s) = \frac{1}{r_1} \quad \text{and} \quad y_{2e}(s) = K_0
\]

These gains do not contain poles or zeros provided that all of the states in the switching cell operate in DCM. This covers most of the known single-switch schemes. In general, for buck and boost rectifiers based on DCM or ZCS/ZVS resonant switches, \( y_{22}(s) \) and \( y_{2e}(s) \) would be frequency-independent and found from the dc characteristics. It should be mentioned that this is line-frequency averaged model and that variation in duty cycle \( D \) must be slow compared to line frequency.

Fig. 10 shows the plot of the predicted normalized ac resistor \( r_1 / R \) versus the converter operating point \( M \) for the rectifier of Fig. 7, the ac resistor \( r_1 \) approaches the lead resistor \( R \) for high values of \( M \).

B. Selection of Output Capacitor \( C_F \)

The selection of the output capacitor \( C_F \) depends on the amount of ripple in the output voltage. The output voltage ripple can be evaluated by integrating the capacitor current,

\[
i_c = C_F \frac{dV_{CF}}{dt}
\]

and the peak ripple can be defined,

\[
\Delta V_{CF}(t) = \frac{1}{C_F} \int_{t}^{t+\pi/3} i_c \, dt, \quad t \in \left[ 0, \frac{\pi}{3\omega} \right]
\]

\[
= \frac{1}{C_F} \int_{0}^{\pi/12} (i_{dK} - I_o) \, dt
\]

Fig. 9: \( Y \)-parameter model for the dc-port of single switch rectifier.

Fig. 10: Predicted ac resistor vs. the converter operating point \( M \).

Where from Fig. 8, the current \( i_{dK} \) can be expressed by

\[
i_{dK} = (d_{1K} + m_{1K})(-i_{1K})
\]

\[
= -(d_{1K} + m_{1K}) \frac{D_T}{2L} v_b(t_k)
\]

and \( d_{1K} + m_{1K} \) is given by (16). Evaluating (30) one can obtain,

\[
\Delta V_{CF}(t) = K_4 \int_{0}^{\pi/12} \frac{(v_b(t) - v_c(t))}{(v_b(t) - v_c(t) + V_o)} v_b(t) \, d(\omega t) - \frac{V_o}{4RC_F}
\]

where

\[
K_4 = \frac{D_o^2 T_s}{8L C_F}
\]

The peak voltage ripple \( V_{ip} \) can be calculated from (32) as,

\[
V_{ip} = K_4 \int_{0}^{\pi/12} \frac{(v_b(t) - v_c(t))}{(v_b(t) - v_c(t) + V_o)} v_b(t) \, d(\omega t) - \frac{V_o}{4RC_F}
\]

and the peak-peak ripple \( V_{ip-p} \) is

\[
V_{ip-p} = 2V_{ip}
\]

To confirm some of the results obtained in this section, the rectifier of Fig. 7, has been simulated for a power level of 920W with the following circuit parameters: \( V_{1K}=86.6\, V_m \) @ 60Hz, \( V_d=262.7V \), \( C_p=100\mu F \), \( L=65\mu H \), \( C_c=25k\mu F \), \( D_o=0.5015 \) and \( R=75\Omega \). Fig. 11, shows the simulated output voltage \( v_{o} \). The peak-peak voltage ripple form Fig. 11, is about 2.85V while evaluating \( V_{ip-p} \) form (33) yields 2.78V. Furthermore, evaluating the coefficient \( B \) in (24) yields \( B=47.39 \) while numerical evaluation of \( B \) from (23) (by mathematica) gives the value of 45.86. Thus, both theoretical and simulation results are in a good agreement.
V. CONCLUSIONS

The concept of one-cycle control is applied to the 3ϕ high quality rectifiers utilizing a single controllable switch. The controller partially reduces the line harmonic currents, and produces a well-regulated dc output voltage. The implementation of the control circuit is simple when compared to the conventional 3ϕ ac-dc six switch rectifiers. Other advantages over the conventional feedback control are obtained such as good dynamic response and good line harmonic rejection. While it retains the advantages of the conventional feedback technique such as stability of the control loop and correction of errors introduced by switch conduction losses and delays.

A small signal averaged ac-model is derived for the 3ϕ ac-dc DCM boost rectifier which can be extended to other rectifiers falling in this class. A Y-parameter model is derived for the dc-side of the 3ϕ ac-dc single-switch boost rectifier. This model is good for most of the single switch schemes. The results of the theoretical analysis are verified by simulation. A good consistency of the results has been found.

REFERENCES