Abstract - A nonlinear control loop mapping has been designed for mitigating the dead zone of a noninverting buck-boost converter while minimizing state variable perturbation. This paper derives a new nonlinearity which enables a converter with fixed switching frequency to achieve reduced switching loss, as though operating at an effective switching frequency lower than the actual. The new control loop nonlinearity accomplishes this by interleaving a specified fraction of pass-through and non-pass-through switching periods. The derived nonlinearity also reduces the increase in waveform ripple associated with a switching frequency reduction. By adapting the effective switching frequency across the full range of conversion ratios and loads, reductions in loss up to 58% are realized.

Index Terms - DC-DC power converters, adaptive switching frequency, buck-boost converter, dead zone, digital control

I. INTRODUCTION

Numerous power electronics applications exist in which the ability to selectively buck or boost the input signal voltage is required. A number of converters exist which can provide both conversion capabilities. Among these, the synchronous form of the noninverting buck-boost (NIBB) converter, shown in Fig. 1, compares favorably in applications requiring the highest possible efficiency [1]-[9]. As seen in Fig. 1 the NIBB converter has separate buck and boost duty cycle controls, which together set the conversion ratio according to

\[ \frac{V_2}{V_1} = \frac{D_{\text{Buck}}}{1 - D_{\text{Boost}}} \]  

(1)

If \( D_{\text{Boost}} = 1 - D_{\text{Buck}} = 0 \) then \( Q_1(Q_2) \) and \( Q_4(Q_3) \) are permanently on (off) and \( V_2/V_1 = 1 \). This “pass-through” mode theoretically offers the highest possible efficiency and is appealing for applications, such as photovoltaic (PV) optimizers and microinverters, in which bucking or boosting might not always be necessary.

The primary disadvantage of the NIBB converter involves the presence of an operational dead zone near the interface between its buck and boost modes. This dead zone creates a region of poor regulation and potential instability and is caused by the necessary insertion of turn-on delay by the Dead Time Generators (DTGs) and by unavoidable on/off state toggling delay differentials [10]. The existence of the NIBB dead zone has long been acknowledged with a number of techniques proposed for dealing with it [3]-[20].

Most recently, [10] has proposed a dead zone avoidance and mitigation (DZAM) processor as the solution to the dead zone problem. As illustrated in Fig. 2, this technique features the insertion of a nonlinear functional mapping between the compensator and Digital Pulse Width Modulator (DPWM) of a digital control loop. As discussed in detail below, the DZAM nonlinear mapping solves the NIBB dead zone problem, and in this paper is generalized to increase converter efficiency through adaptation of its switching loss characteristics.

The DZAM nonlinear mapping of Fig. 2 is implemented as part of the Digital Signal Processing (DSP) required for a digital controller. With the advent of very inexpensive DSP microcontrollers, sophisticated digital control of 100-500 kHz PWM converters has become practical. These microcontrollers typically exhibit 30-100 MHZ clock frequencies with hardware multipliers, and contain useful control peripherals such as
allows the DZAM nonlinear mapping shown in Fig. 2 to be double the switching loss. The exception to this is at , amounts that keep all four FETs toggling, while maintaining the desired conversion ratio 

Fig. 2 that DPWM maps each input value \( q \) to a corresponding buck and boost duty cycle value \( (d_{\text{Buck},n}, d_{\text{Boost},n}) \) according to the curves of Figures 3-4. Fig. 3 handles the case \( q \notin (MZ_u, MZ_o) \), where the DPWM dynamic range is \([-M, M]\), and the dead zone is denoted \( q \in (MZ_u, MZ_o) \) where \( -Z_u \) and \( Z_o \) are positive fractions less than 1 and typically << 1. The curves of Fig. 4 address the case \( q \notin (MZ_u, MZ_o) \). Fig. 4 avoids the dead zone regulation problem by increasing \( d_{\text{Boost},n} \) and decreasing \( d_{\text{Buck},n} \) by amounts that keep all four FETs toggling, while maintaining the desired conversion ratio [10]. Since the curves of Fig. 4 produce both \( d_{\text{Boost}} > 0 \) and \( d_{\text{Buck}} < 1 \), \( q \in (MZ_u, MZ_o) \) produces a tri-interval switching period, i.e., one with three conduction intervals instead of the normal two, and therefore double the switching loss. The exception to this is at \( q = 0 \), which yields \( d_{\text{Boost}} = 1 - d_{\text{Buck}} = 0 \) and hence no switching and no switching loss.

The DZAM processor in Fig. 2 produces a DPWM input sequence which either cancels the doubling of switching loss resulting from any tri-interval periods or disallows \( q \notin (MZ_u, MZ_o) \) completely. The sequence \{\( q_n \}\) output by the DZAM processor also maintains the desired conversion ratio while minimizing the perturbation to converter state variables resulting from \{\( q_n \}\} \neq \{\( p_n \}\}. Unlike prior techniques, DZAM solves the dead zone problem without increasing switching loss and without the need for mode changes which place restrictions on converter I/O signal bandwidth. As derived in [10], the DZAM processor structure which accomplishes this is shown in Fig. 5. The DZAM processor contains a memoryless nonlinearity \( f_{\text{DZ}}(x_n, e_{n-1}) \) which maps an input point \( x_n \) within the dead zone to a new output point \( q_n \), while passing input points outside the dead zone unmodified to the output. The behavior and performance of the DZAM technique are determined by the exact form for \( f_{\text{DZ}}(\cdot) \), with 4 different nonlinearities designed in [10] and [21] for specific desired characteristics. The remaining portions of the DZAM processor zero out the accumulated error \( e_n \) between the sequences \{\( q_n \}\} and \{\( p_n \}\) whenever a nonlinearity input \( x_n \) outside the dead zone occurs. In [10] it is shown that a DZAM processor has some similarity to a first order \( \Sigma \Delta \) modulator, but with the important difference that \( f_{\text{DZ}}(\cdot) \) need not simply quantize \( x_n \) in forming \( q_n \). This difference enables the design of DZAM nonlinearities which can impart a wide variety of behavioral characteristics to the duty cycle sequence \{\( (d_{\text{Buck},n}, d_{\text{Boost},n}) \}\}. This generalized nature of \( f_{\text{DZ}}(\cdot) \) is exploited both in the dead zone mitigation application of [10] and in the application developed here. In this paper, the DZAM processor concept is extended to the maximization of buck-boost converter efficiency via implementation of an adaptive effective switching frequency. The operational efficiency of a given NIBB converter implementation is a function of switching frequency \( f_s \), load current, and conversion ratio \( V_2/V_1 \). For a given load current, efficiency can be plotted vs. conversion ratio as a family of curves, with each curve representing a particular
Section II of this paper describes techniques in the existing literature for automatically selecting and adapting the value of switching frequency in an attempt to increase converter efficiency. This paper focuses instead on the related but separate question of how best to implement the multiple switching frequencies called for by a given efficiency optimizing scheme. In the case where a digital controller is assumed, Section II describes the additional DSP which must be performed to accommodate an adaptive switching frequency. While theoretically straightforward, this additional processing adds to the cost and quiescent power consumption of the converter, which will preclude its use in many applications.

In response, this paper proposes to use the DZAM processor to produce a converter with an adaptive effective switching frequency. In particular, a converter is proposed in which the switching and DSP sampling frequencies remain fixed and equal, but whose switching loss can nevertheless be reduced to any desired level. As described in Section II, this is accomplished by interleaving pass-through switching periods with non-pass-through periods in an optimal fashion. As pass-through periods involve no switching or switching loss, the average value of switching loss can be controlled by varying the total fraction of pass-through periods. While the converter switching frequency is fixed at a nominal value $f_{s,nom}$, the amount of switching loss can be set to equal that which would occur for a traditional converter with any fixed switching frequency equal to $f_{s,eff} = f_{s,nom}$.

Section III of this paper describes the new DZAM nonlinearity which accomplishes this optimal interleaving of pass-through and non-pass-through switching periods. In addition to providing a given desired value for $f_{s,eff}$, the resulting DZAM nonlinear mapping maintains the conversion ratio associated with $\{p_n\}$ while minimizing the norm of the accumulated input/output error sequence. This latter characteristic approximates the goal of minimizing the increase in waveform ripple that by necessity accompanies any decrease in switching frequency. Section IV evaluates the degree of success achieved by this approximation, by comparing the inductor current peak and rms values associated with the DZAM nonlinearity to that of a baseline converter with fixed switching frequency equal to $f_{s,eff}$. As shown in Section IV, the result is that for cases in which $f_{s,eff}$ divides $f_{s,nom}$, the two inductor current waveforms are equal, and hence no additional ripple increase due to DZAM occurs. For cases in which $f_{s,eff}$ does not divide $f_{s,nom}$, a < 1% increase in rms inductor current occurs for the DZAM technique, but increases in inductor current peak can be much larger, as high as 24%. Section IV describes the source of this apparent discrepancy, and notes that it is addressed by biasing switching frequency selection away from the specific $f_{s,eff}$ values with the largest peak increases.

**Fig. 6.** Converter efficiency vs. conversion ratio for fixed load and two different fixed switching frequencies (solid). Dashed curve is efficiency at optimal switching frequency, adapted for each conversion ratio.

fixed switching frequency. An illustrative example appears in Fig. 6, in which the efficiencies vs. conversion ratio for two fixed switching frequencies $f_{s1} > f_{s2}$ are shown as the two solid curves. Both curves will exhibit a spike in efficiency at $V_2/V_1 = 1$ if this unity conversion ratio is implemented as a pass-through mode with $D_{Boost} = 1 - D_{Buck} = 0$, since in this case no switching and no switching loss occurs.

As illustrated in Fig. 6, the onset of switching for $V_2/V_1 \neq 1$ produces an unequal step down in efficiency, proportional to the fixed switching frequency in use. For both switching frequencies the efficiency decreases smoothly as the system moves away from pass-through, but efficiency for the lower switching frequency curve decreases more rapidly. The reason is that, for a fixed load current, inductor current ripple, peak, and rms values all increase with the operating distance from pass-through, with the increase in these quantities occurring more rapidly at lower switching frequency. Taken together, these two phenomena mean that the efficiency-maximizing switching frequency is zero at unity conversion ratio, and increases monotonically in both buck and boost modes as the distance from pass-through increases. A corresponding plot of efficiency vs. conversion ratio for a NIBB converter which optimally adapts its switching frequency would thus assume the form illustrated by the dashed curve of Fig. 6.

The pass-through efficiency spike of Fig. 6 can be demonstrated with a fixed switching frequency converter “running” (with no switching) open-loop. However, in normal closed loop operation the average efficiency of a fixed switching frequency converter cannot approach the spike maximum. The reason is that jitter/wander in the control loop, and any perturbation to the control loop reference signal $v_{ref}$, mean that, at best, the converter will spend a small fraction of time in pass-through during steady state. Average efficiency in this best case will be, for example, 1% of the spike efficiency plus 99% of the values averaged just below the spike. By contrast, a NIBB converter which optimally adapts its switching frequency will achieve the dashed efficiency curve of Fig. 6, including actual steady state realization of the maximum value near pass-through.
Section V presents experimental results for a PV converter which demonstrate the interleaving of pass-through and non-pass-through periods and the corresponding impact on measured efficiency. The results demonstrate that unrealizable steady state operation at a pass-through efficiency spike is transformed into realizable operation near a pass-through efficiency maximum, with peak reductions in loss as high as 58% recorded. Section VI provides a summarizing conclusion.

II. SPECIFICATION AND IMPLEMENTATION OF A VARIABLE SWITCHING FREQUENCY

The use of an adaptive switching frequency to increase converter efficiency has received considerable attention in the literature [22]-[40]. Of particular interest is the buck converter for portable battery-operated devices, such as cell phones, which operate most of the time in a standby state. Maximizing converter efficiency at very light load is critical to extending battery life in such applications. As a result, most of the literature is focused on automatically reducing the switching frequency and switching losses at light load.

Various criteria have been established for automatically setting the time-dependent value of switching frequency, \( f_s(t) \), in such systems. In [22]-[26] \( f_s(t) \) is driven by a perturb and observe algorithm which minimizes the converter input power. Another common approach is to scale \( f_s \) linearly or nonlinearly with load current, but only when operating at light load in Discontinuous Conduction Mode (DCM) [27]-[32]. In [33]-[36] \( f_s(t) \) is set so as to achieve zero voltage switching, and therefore increased efficiency, over the widest possible range of load currents. In [37]-[40] \( f_s(t) \) is set to deliver some function of the inductor current peak and/or ripple magnitude value. Notice that, as in Fig. 6, this final criteria will adapt the switching frequency as the conversion ratio changes even when the load current remains fixed. As converter efficiency is a function of load current, \( V_2/V_1 \), and \( f_s \), an ideal implementation will optimize switching frequency as a function of both conversion ratio and load.

In this paper the emphasis is not on the specification of \( f_s(t) \), but rather on a new DZAM-based technique for implementing the multiple switching frequencies called for by a given \( f_s(t) \) function. Development of this technique is a response to the challenges associated with implementing an adaptive switching frequency with a digital controller. As pointed out in [41], discrete-time generation of an adaptive switching frequency produces a wide-ranging set of values for the DPWM gain. This makes the values for loop gain bandwidth and stability margin functions of switching frequency, and also increases the dynamic range requirements for the digital controller. DPWM resolution is similarly affected, which means that ADC resolution may require switching frequency-dependent adaptation in order to avoid limit cycling behavior [22],[41]. Dead zone boundaries and tri-interval duty cycles values will also require continual switching frequency-dependent adjustment [10]. In addition, this paper will show that maximization of NIBB converter efficiency can require a ratio of maximum-to-minimum switching frequencies as high as 32. In order to maintain control loop functionality over such a wide range, it is necessary to decouple the switching and ADC/DSP sampling frequencies. This in turn requires the insertion of an interpolating sample rate converter between the control loop compensator and DPWM. All of these challenges are readily addressed, e.g., through the use of multi-rate DSP techniques [42], provided sufficient DSP processing power is available. However, a powerful DSP decreases converter efficiency and increases cost and at present is not suitable in a great many power electronics applications.

The need for an adaptive switching frequency converter with low-complexity digital controller thus motivates the design of a system in which the switching and sampling frequencies are both fixed and equal, but whose switching loss can nevertheless be reduced to any desired level. This paper proposes a system, based on the DZAM processor of Fig. 5, wherein this can be accomplished. The technique involves a windowing of the time axis, with each window containing controlled numbers of interleaved pass-through and non-pass-through switching periods.

An illustrative example is shown in Fig. 7, where \( N_p \) and \( N_s \) denote the number of pass-through and non-pass-through switching periods, respectively, within the window. Each switching period is of duration \( T_s = 1/f_s,nom \), but the values of \( N_p \) and \( N_s \) can change from one window to the next. Fig. 7 is purely illustrative, in that the assignment of window slots to pass-through and non-pass-through periods has a strong influence on performance, with the optimal choice derived in Section III. Because no switching or switching loss occurs during pass-through periods, the switching loss averaged over the course of the window is equal to that of a converter with fixed switching frequency equal to \( f_{s,eff} \)

\[
f_{s,eff} = \frac{N_s}{(N_s + N_p)T_s} = \frac{f_{s,nom}}{N_s + N_p} \tag{2}
\]

This paper designs a new DZAM nonlinearity \( f_{DZ}(x) \) in which the DZAM processor output \( \{q_n\} \) is constrained to provide an interleaved window structure similar to that of Fig.

![Fig. 7. Structure of an example switching period interleaving window](image-url)
Replacing \( \{p_n\} \) in Fig. 2 and Fig. 5 with \( \{q_n\} \neq \{p_n\} \) has the potential to perturb converter state variables in ways which increase waveform ripple. In fact, as in systems where the actual switching frequency itself is reduced below \( f_{s,\text{nom}} \), a corresponding increase in waveform ripple will by necessity result from this technique. The goal in Section III is to design the optimal window interleaving pattern, and the specific sequence \( \{q_n\} \) which implements it, without modifying the desired conversion ratio and while increasing ripple by the minimum possible amount. As increasing ripple increases conduction and magnetics losses, the ideal sequence \( \{q_n\} \) would deliver the switching loss associated with a specified value of \( f_{s,\text{eff}} \) while also minimizing the associated increase in conduction and magnetics losses. Section III implements an approximation to this ideal \( \{p_n\}\)-to-\( \{q_n\} \) map through the design of a new nonlinearity for the DZAM processor.

III. DZAM ADAPTIVE EFFECTIVE SWITCHING FREQUENCY NONLINEARITY

This section derives the DZAM nonlinearity which delivers a given effective switching frequency \( f_{s,\text{eff}} \leq f_{s,\text{nom}} \) while approximating the goal of minimal corresponding increase in conduction and magnetics losses. As the exact solution to this goal is currently unknown, this section derives instead the nonlinearity which minimizes the \( L_2 \) norm of the DZAM accumulated error sequence \( e_n \), \( 1 \leq n \leq N_s+N_p \), over the course of the window. It is shown in [10] that the increase in inductor current ripple due to DZAM is proportional to this norm, and hence this design approach serves as an approximation to the ideal goal.

This approximate solution is derived in two steps. Section III.A derives the value of the \( L_2 \)-minimizing subsequence of DZAM outputs \( \{q_n\} \) corresponding to the set of \( N_s \) non-pass-through periods, for \( (N_s,N_p) \) and the location of each such period considered given. Section III.B then derives the location for the \( N_s \) non-pass-through periods within the window that minimizes \( L_2(\{e_n\}) \).

A. Optimization of Non-Pass-Through Period Values for \( \{q_n\} \)

In this section we are given \( (N_s,N_p) \) and the locations for the \( N_s \) non-pass-through periods within the window. With reference to Fig. 5, we then derive the sequence \( \{q_n\} \) which minimizes \( L_2(\{e_n\}) \) over the window-length time indices \( n = 1, 2, \ldots, N_s+N_p \). Denote the subset of these time indices which point to non-pass-through periods as the set \( N_s = \{i_1, i_2, \ldots, i_{N_s}\} \) where

\[
1 = i_1 < i_2 < \ldots < i_{N_s} \leq N_s+N_p \quad (3)
\]

The quantity \( i_p 1 \leq l \leq N_s \), denotes the time index within the current window during which the \( l \)th non-pass-through switching period occurs. The specification of \( i_1 = 1 \) is justified shortly. The accumulated error left over from DZAM processing during the previous window is denoted \( e_0 \). Denote \( c_l \geq 0 \) as the number of consecutive pass-through periods which follow the \( l \)th non-pass-through switching period. With this construction we have

\[
i_1 = 1; i_{j+1} = i_j + c_j + 1 = l + 1 + \sum_{k=1}^l c_k; l = 1, \ldots, N_s - 1 \quad (4)
\]

Since pass-through periods are implemented with \( q_n = 0 \),

\[
q_{i_j + m} = 0; l = 1, 2, \ldots, N_s; m = 1, 2, \ldots, c_l \quad (5)
\]

By writing out the first few terms in Fig. 5 starting with \( n = 1 \) we can see that

\[
x_n = -e_0 + p_n + \sum_{k=1}^{n-1} (p_k - q_k) \quad (6)
\]

\[
e_n = e_0 + \sum_{k=1}^n (q_k - p_k) \quad (7)
\]

From (5) and (7) we have that

\[
e_{i_j + m} = e_{i_j} - \sum_{k=1}^m p_{i_j + k}; l = 1, 2, \ldots, N_s; m = 0, 1, \ldots, c_l \quad (8)
\]

Equation (8) is plotted in Fig. 8, which as shown is linear for the case \( p_{i_j + 1} = p_{i_j + 2} = \ldots = p_{i_j + c_l} \). As seen in both (8) and Fig. 8 the value of the subsequence \( \{e_{i_j}, e_{i_j + 1}, \ldots, e_{i_j + c_l}\} \) is set solely by \( e_{i_j} \) and the input sequence values

![Fig. 8. Error subsequence \( \{e_{i_j}, e_{i_j + 1}, \ldots, e_{i_j + c_l}\} \) drawn linear for the case \( p_{i_j + 1} = p_{i_j + 2} = \ldots = p_{i_j + c_l} \)]
\{p_{i+1}, p_{i+2}, \ldots, p_{i+c_i}\}$ \). The DZAM algorithm has no control over the input sequence, but does control the value of $e_{i_j}$ by way of
\[ e_{i_j} = e_{i_j-1} + q_{i_j} - p_{i_j} = p_{i_j} + e_{i_j-1} = x_{i_j} + e_{i_j} \quad (9) \]

Hence given the residual error $e_{i_j-1}$ at the end of the preceding error subsequence, the starting point for the current error subsequence can be controlled by the DZAM algorithm using (9). As a result the rms value of the error sequence within the entire window $\{e_1, e_2, \ldots, e_{N_s+N_p}\}$ can be minimized by separately and independently minimizing the rms value of each of the $N_s$ subsequences $\{e_{i_1}, e_{i_2}, \ldots, e_{i_{N_s}}\}$, $l = 1, 2, \ldots, N_s$. Such is the approach taken here. Note that the approach requires setting $i_1 = 1$, otherwise the terms $\{e_1, e_2, \ldots, e_{i_1}\}$ are either left out of the minimization, or are included through the setting of the value for $q_{i_N}$ during the previous window. The former approach fails to minimize the rms value of the entire error sequence, and the latter approach violates causality, as knowledge of the parameters for future windows is not yet available. We conclude that $i_1 = 1$.

The rms value of the $l$th subsequence is minimized by minimizing the quantity
\[ r^*_l = \sum_{m=0}^{c_l} \frac{e_{i_j+m}^2}{2} \sum_{m=0}^{c_l} \left( e_{i_j+m} - \frac{p_{i_j+m}}{2} \right)^2 \quad (10) \]

where the second equality is due to (8). Since
\[ \frac{dr^*_l}{de_{i_j}} = 2e_{i_j}(1+c_l) - 2 \sum_{m=0}^{c_l} \sum_{j=1}^{m} p_{i_j+j} \quad (11) \]

the value of $e_{i_j}$ which minimizes the rms value of $\{e_{i_1}, e_{i_2}, \ldots, e_{i_{N_s}}\}$ is
\[ e_{i_j} = \frac{1}{1+c_l} \sum_{m=0}^{c_l} \sum_{j=1}^{m} p_{i_j+j}, \quad l = 1, 2, \ldots, N_s \quad (12) \]

Substituting (12) in (9) the corresponding DZAM filter output is
\[ q_{i_j} = x_{i_j} + \frac{1}{1+c_l} \sum_{m=0}^{c_l} \sum_{j=1}^{m} p_{i_j+j}, \quad l = 1, 2, \ldots, N_s \quad (13) \]

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{fig9.pdf}
\caption{Minimum $L_2$ norm $f_{n,e_{n-1}}$ adaptive $f_{n,e_{n-1}}$ DZAM processor}
\end{figure}

Note, however, that computation of $q_{i_j}$ via (13) violates causality because the right hand side includes $\{p_{i_j+1}, p_{i_j+2}, \ldots, p_{i_j+c_l}\}$. If instead we accept the approximation
\[ p_{i_j} \approx p_{i_j+1} \approx \cdots \approx p_{i_j+c_l} \quad (14) \]

and treat it as an equality, (13) becomes implementable as
\[ q_{i_j} = x_{i_j} + p_{i_j} \left( 1 + \frac{c_l}{2} \right) - e_{i_j-1}, \quad l = 1, 2, \ldots, N_s \quad (15) \]

for which case Fig. 5 and (15) yield
\[ e_{i_j} = e_{i_j-1} + q_{i_j} - p_{i_j} = p_{i_j} c / 2 \quad (16) \]

The DZAM processor block diagram of Fig. 5 is updated in Fig. 9 to reflect the optimal implementable filter output described by (5) and (15). As shown in [21], the nonlinearity of Fig. 5 corresponding to (15) is given by
\[ f_{DZ}(x_n, e_{n-1}) = \begin{cases} x_n \left( 1 + \frac{c_l}{2} \right) + \frac{e_{n-1} c_l}{2}; & n = i_t, l = 1, 2, \ldots, N_s \\ 0; & n \neq i_t \end{cases} \quad (17) \]

which shows that the nonlinearity for this case is actually a time-varying linearity.

**B. Optimal Location for the $N_s$ Non-Pass-Through Periods**

Substituting (16) in (11) the optimal implementable error sequence
\[ e_{i_j+m} = p_{i_j+m} - \sum_{j=1}^{m} p_{i_j+j}, \quad l = 1, 2, \ldots, N_s; \quad m = 0, 1, \ldots, c_l \quad (18) \]

For the constant input case $p_n = p$, $\forall n$, (18) becomes
\[ e_{i_j+m} = p_{i_j+m} - m; \quad l = 1, 2, \ldots, N_s; \quad m = 0, 1, \ldots, c_l \quad (19) \]

The $L_2$ norm of $\{e_1, e_2, \ldots, e_{N_s+N_p}\}$ for the constant input case is thus
Minimization of (20) occurs by spreading the $N_s$ non-pass-through periods throughout the window as uniformly as possible. Hence the set \( \{c_1, c_2, \ldots, c_{N_s}\} \) of nonnegative integers which minimizes (20), subject to the constraint
\[
\sum_{l=1}^{N_s} c_l = N_p
\]
is given by
\[
c_l = \left[ \frac{M_p(l)}{M_s(l)} \right]; \quad l = 1, 2, \ldots, N_s
\]
(22)
where \( \lfloor x \rfloor \) is the smallest integer \( \geq x \). \( M_p(l) \) and \( M_s(l) \) are by definition the total number of pass-through periods and non-pass-through periods, respectively, remaining within the window measured from and including the current switching period \( n = i_l \). \( M_s(l) \) is simply
\[
M_s(l) = N_s - l + 1; \quad l = 1, 2, \ldots, N_s
\]
while \( M_p(l) \) is given recursively by
\[
M_p(1) = N_p; \quad M_p(l+1) = M_p(l) - c_l; \quad l = 1, 2, \ldots, N_s - 1
\]
(24)
For given values of \((N_s, N_p)\), the location for the \(N_s\) non-pass-through switching periods within the window is given by (4) and (22)-(24). For implementation purposes [21] proves that
\[
c_l - c_{l+1} \in \{0, 1\}
\]
(25)
For the constant input case \( p_n = p \) we have from (19) that
\[
e_{i_l} + c_l = -e_{i_l} = -pc_l/2, \quad l = 1, 2, \ldots, N_s
\]
(26)
Hence for the constant input case the solution of this section also minimizes the \( L_2 \) norm
\[
\max_n \left| e_n \right|
\]
IV. CONVERTER CHARACTERISTICS FOR DZAM-BASED ADAPTIVE EFFECTIVE SWITCHING FREQUENCY
This section evaluates the NIBB converter steady state conversion ratio and inductor current characteristics when driven by the adaptive \( f_{s, eff} \) DZAM processor of Fig. 9, in combination with the DPWM curves of Figures 3-4.

A. Conversion Ratio
In this section we assume that \( f_{s, eff} \leftrightarrow (N_s, N_p) \) and \( p_n = p \) are both constant, in which case \( \{q_n\} \) and all converter waveforms are periodic with period \( (N_s + N_p)T_s \). As shown in [21] the conversion ratio in this case is given by
\[
\frac{V_2}{V_1} = \frac{d_{Buck}}{1 - d_{Boost}}
\]
(27)
where
\[
d_{Buck} = \frac{1}{(N_s + N_p)} \sum_{n=1}^{N_s + N_p} d_{Buck,n}
\]
(28)
\[
d_{Boost} = \frac{1}{(N_s + N_p)} \sum_{n=1}^{N_s + N_p} d_{Boost,n}
\]
(29)
are the buck and boost duty cycles averaged over the course of the window, and where the result of (1) for \((N_s = 1, N_p = 0)\) is seen to be a special case of (27). In [21] it is shown that if \( p \) is such that one or more values of \( \{q_{i_l}\} \) fall within the dead zone, the resulting \( (d_{Buck}, d_{Boost}) \) may be such that a very small error (< 0.07%) in conversion ratio occurs, compared to the case for the same value of \( p \) with \( f_{s, eff} = f_{s, nom} \). If all members of \( \{q_{i_l}\} \) fall outside the dead zone the conversion ratio error is exactly zero.

B. Inductor Current RMS and Peak Values
A combination of closed form and numerical analysis is applied in [21] in the determination of the inductor current waveform, for a given average load current, generated by the DZAM-based adaptive \( f_{s, eff} \) technique of this paper. In this section the rms and peak values of that waveform are compared to that of a baseline system with fixed switching frequency equal to \( f_{s, eff} \). Both systems use the bi/tri-interval DPWM curves of Figures 3-4. For both DZAM-based and baseline systems, inductor current peak and rms values will increase as \( f_{s, eff} \) is decreased and as the assumed constant compensator output value \( p \) increases in absolute value. The intent of this section is to evaluate the additional increase in peak and rms values which occurs with the DZAM-based technique, relative to that of the baseline system.

Numerical results are generated for an example system with output voltage \( V_2 \) regulated at 50V, 5 amp load current, \( f_{s, nom} = 100 \text{ kHz} \), \( M = 960 \), \( MZ_o = -MZ_u = 48 \), and \( L = 27 \mu \text{H} \). For study purposes within this section only, \( N_s + N_p \) is fixed at 32, and \( N_s \) is varied between 1 and 32. The results for increase in rms and peak values of inductor current are shown in Figures 10-11 and Figures 12-13, respectively. Each of these figures exhibits markedly different behavior inside and outside of the dead zone (-48,48). The
reason is that for all \( p \) inside the dead zone, the baseline system with fixed \( f_s = f_{s,\text{eff}} \) always operates in tri-interval mode. By contrast, the DZAM processor maps the constant input \( p_n = p \in (MZ_{w_p}M_{Z_p}) \) to a sequence \( \{q_n\} \), which, in general, may contain a complex combination of bi-interval, tri-interval, and pass-through points. Inside the dead zone many of the curve points in Figures 10-13 are negative, at which points the increase in \( i_L \) for the DZAM technique is actually less than that for the baseline system. This occurs because tri-interval operation not only doubles switching loss but also increases \( i_L \) due to the associated increase in \( d_{\text{Boost}} \) (see Fig. 4). For conditions within the dead zone in which DZAM does increase \( \text{rms}(i_L) \) and/or \( \text{peak}(i_L) \), the increases are small compared to outside the dead zone. Hence our primary interest is in increases outside the dead zone.

From Figures 10-11 we see that for \( |p| \leq 140 \) the additional increase in \( \text{rms}(i_L) \) due to DZAM outside the dead zone is less than 0.9%. However, from Figures 12-13, the additional increase in \( \text{peak}(i_L) \) over the same range can be as high as 24%, a far larger figure. As described in [21], this discrepancy arises in situations where the selected value of \( (N_s,N_p) \) results in a maximum distance between non-pass-through periods well in excess of that for the baseline system case. At some values of \( (N_s,N_p) \) this is an unavoidable consequence of the discretization of the time axis associated with the use of a fixed \( T_s \). The increased values for \( \text{peak}(i_L) \) seen in Figures 12-13 are produced by the fact that, during the intervening pass-

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**Fig. 10.** Percent increase in \( \text{rms}(i_L) \) vs. \( p \) for DZAM-based adaptive effective switching frequency \( f_{s,\text{eff}} = f_{s,\text{nom}}N_s/32 \) for \( N_s = 1, 2, \ldots, 16 \), relative to baseline system with fixed \( f_s = f_{s,\text{eff}} \)

**Fig. 11.** Percent increase in \( \text{rms}(i_L) \) vs. \( p \) for DZAM-based adaptive effective switching frequency \( f_{s,\text{eff}} = f_{s,\text{nom}}N_s/32 \) for \( N_s = 17, 18, \ldots, 32 \), relative to baseline system with fixed \( f_s = f_{s,\text{eff}} \)

**Fig. 12.** Percent increase in \( \text{peak}(i_L) \) vs. \( p \) for DZAM-based adaptive effective switching frequency \( f_{s,\text{eff}} = f_{s,\text{nom}}N_s/32 \) for \( N_s = 1, 2, \ldots, 16 \), relative to baseline system with fixed \( f_s = f_{s,\text{eff}} \)

**Fig. 13.** Percent increase in \( \text{peak}(i_L) \) vs. \( p \) for DZAM-based adaptive effective switching frequency \( f_{s,\text{eff}} = f_{s,\text{nom}}N_s/32 \) for \( N_s = 17, 18, \ldots, 32 \), relative to baseline system with fixed \( f_s = f_{s,\text{eff}} \)
through periods, $i_L$ slopes up or down at the constant rate of $(V_1 - V_2)/L$.

This phenomenon is quantified as the ratio of the maximum distance between non-pass-through periods for the DZAM-based technique, divided by the baseline system switching period, given by

$$\rho_{\text{max}} = \frac{(1 + c_1)T_s}{1/f_{s,\text{eff}}} = \frac{1 + \lceil N_p/N_s \rceil}{1 + (N_p/N_s)}$$  \hspace{1cm} (30)

where the second equation results from substituting (2) and (22)-(24). Due to the definition of $[x]$, notice that

$$1 \leq \rho_{\text{max}} < 1 + \frac{N_p}{N_s + N_p}$$  \hspace{1cm} (31)

with the lower bound achieved only for $(N_s, N_p)$ satisfying

$$\frac{N_s}{N_s + N_p} = \frac{1}{K} \leftrightarrow f_{s,\text{eff}} = \frac{f_{s,\text{nom}}}{K}, \text{ K any positive integer}$$  \hspace{1cm} (32)

As shown in (32), values for $(N_s, N_p)$ satisfy (32) when $f_{s,\text{eff}}$ divides $f_{s,\text{nom}},$ in which case the DZAM and baseline system inductor current waveforms are identical, $\rho_{\text{max}} = 1,$ and the DZAM technique imparts no additional increase to peak($i_L$) relative to that from the baseline system. For converters with loss characteristics sensitive to peak($i_L$), the results of this section indicate that efficiency optimization algorithms using the DZAM-based technique will exhibit a bias towards the selection of effective switching frequencies which satisfy (32), followed by those for which $\lceil N_p/N_s \rceil$ is only slightly greater than $(N_p/N_s).$

V. EXPERIMENTAL RESULTS

A. Experimental Setup

This section presents experimental results generated with a DZAM-based adaptive effective frequency $f_{s,\text{eff}}$ NIBB converter, which functions as part of a power converter for a parallel PV architecture. The converter parameters are $T_s = 1/f_{s,\text{nom}} = 9.6\mu s, M = 960, MZ_o = -MZ_o = 48, \text{ and } L = 27 \mu H.$ All control and DZAM processor functionality are implemented on a 16 bit, 32 MHZ Freescale MC56F8006 digital signal controller. The maximum supported value of $N_s + N_p$ is 32, as $f_{s,\text{nom}}/(N_s + N_p)$ must be kept well above the control loop bandwidth in order to keep DZAM “invisible” to the rest of the system. The only other restrictions on $f_{s,\text{eff}}$ are $N_s \geq 1$ and $N_p \geq 0.$

The experimental setup is shown in Fig. 14. The converter is run open loop with a constant DZAM input $P_n = p$ as an independent variable. The converter output is connected to a constant voltage load, regulated at 50V. A voltage source is connected to the input through a 6Ω power resistor, and adjusted for an average output current $I \in \{1, 2, 4\}$ (50W, 100W, and 200W, respectively). The window parameters $(N_s, N_p) \leftrightarrow f_{s,\text{eff}}$ are set as a function of $p$ and $I$ from a lookup table, whose entries have been empirically determined to yield maximum efficiency. In Fig. 15 the resulting value of $f_{s,\text{eff}}/f_{s,\text{nom}}$ is plotted vs. $p$ for $I \in \{1, 2, 4\}.$ As described in Section IV, the discrete steps visible in Fig. 15 arise from the tendency of $f_{s,\text{eff}}$ values which satisfy (32) to yield higher efficiency values than nearby values which do not. In particular, the step from $f_{s,\text{eff}} = f_{s,\text{nom}}/2$ to $f_{s,\text{eff}} = f_{s,\text{nom}}$ reflects the fact that there are no intervening values of $f_{s,\text{eff}}$ which satisfy (32). In addition, it can be shown that $(f_{s,\text{nom}}/2) < f_{s,\text{eff}} < f_{s,\text{nom}} \Rightarrow \rho_{\text{max}} = 2 f_{s,\text{eff}}/f_{s,\text{nom}},$ which means that effective switching frequencies $f_{s,\text{eff}}$ approaching $f_{s,\text{nom}}$ are unlikely to yield good efficiency results. This limitation can be addressed by setting $f_{s,\text{nom}}$ to twice the value of the maximum desired switching frequency, provided the DSP has sufficient power for the increase.

![Fig. 14. Experimental setup for NIBB converter with DZAM-based adaptive effective switching frequency $f_{s,\text{eff}}$.

![Fig. 15. Measured values of $f_{s,\text{eff}}/f_{s,\text{nom}}$ which maximize efficiency, as a function of DZAM input $p$ and load current $I = \text{Power}/(50V).$](image-url)
Fig. 16. Gate drive waveforms and window length indicator for $f_{s,\text{eff}} = f_{s,\text{nom}}/32$, $p = 4$.

Fig. 17. Gate drive waveforms and window length indicator for $f_{s,\text{eff}} / f_{s,\text{nom}} = 4/32$, $p = 11$.

Fig. 18. Gate drive waveforms and window length indicator for $f_{s,\text{eff}} / f_{s,\text{nom}} = 10/32$, $p = 43$.

Fig. 19. Gate drive waveforms and window length indicator for $f_{s,\text{eff}} / f_{s,\text{nom}} = 1/3$, $p = 43$.

Fig. 20. Gate drive waveforms and window length indicator for $f_{s,\text{eff}} / f_{s,\text{nom}} = 11/32$, $p = 43$.

Fig. 21. Gate drive waveforms and window length indicator for $f_{s,\text{eff}} / f_{s,\text{nom}} = 16/32$, $p = 137$.

Fig. 22. Gate drive waveforms and window length indicator for $f_{s,\text{eff}} / f_{s,\text{nom}} = 17/32$, $p = 137$.

Fig. 23. Gate drive waveforms and window length indicator for $f_{s,\text{eff}} / f_{s,\text{nom}} = 31/32$, $p = 137$. 
B. FET Gate Drive Waveforms

This section demonstrates the interleaving of pass-through and non-pass-through switching periods, within a window of length \((N_s+N_p)T_s\), by which DZAM implements an effective switching frequency. Figures 16-23 plot gate drive and window duration indicator waveforms for the following selected values of \(f_s,\text{eff} / f_s,\text{nom}\) in order: 1/32, 1/8, 10/32, 1/3, 11/32, 1/2, 17/32, and 31/32. The wide range of effective switching frequencies possible with \(N_s+N_p\leq32\) is highlighted through the use of a constant time scale (40 µs/div) across all figures. The choice of \(p>0\) for all figures produces boost operation, with \(d_{\text{Buck},n}=1\) for all switching periods.

Extra functionality required to keep the high side gate drive bootstrap capacitor charged produces the occasional toggling visible for \(d_{\text{Buck}}(t)\) when \(D_{\text{Buck}}=1\).

The figures demonstrate how the DZAM nonlinearity of Section III minimizes \(L_2(\{e_n\})\) and ripple by spacing the non-pass-through periods as uniformly as possible within the window. The values 10/32, 1/3, and 11/32 in Figures 18-20 illustrate the case of a \(f_s,\text{eff}\) value which satisfies (32) bracketed closely by two which do not. The values 17/32 and 31/32 in Figures 22-23 illustrate the difference in system behavior which emerges for \(f_s,\text{eff} > f_s,\text{nom}/2\). In summary, Figures 16-23 demonstrate that the system of Fig. 9 delivers the expected adaptive effective switching frequency while minimizing \(L_2(\{e_n\})\).

C. Steady State Efficiency Results

This section presents measured efficiency results using the experimental setup of Fig. 14. Efficiency is measured as a function of the constant DZAM processor input \(p\), at three different converter output powers: 200W, 100W, and 50W. Fixed losses in the converter due to the housekeeping power supply, gate drive circuits, and micro-controller are included in the efficiency measurements at all power levels. At each output power, efficiency curves are generated for three different effective switching frequency approaches. The first approach is labeled “fixed \(f_s,\text{eff}\)” and uses a fixed switching frequency \(f_s,\text{eff} = f_s,\text{nom} = 104\ kHz\) for all values of \(p\) and for all three output powers, with no DZAM, and with the dead zone mitigated by the tri-interval portion of the DPWM shown in Fig. 4.

The second approach is labeled “DZAM dual \(f_s,\text{eff}\)” and applies the tri-interval, two-sample period DZAM technique of [10] for dead zone mitigation alone. As described in [10], in this case a value of \(p\) within the dead zone produces \(f_s,\text{eff} = f_s,\text{nom} / 2\) with pass-through periods alternating with either bi- or tri-interval periods, depending on the value \(q_n = 2p\). Outside the dead zone \(f_s,\text{eff} = f_s,\text{nom}\) and \(q_n = p_n\).
The final approach, labeled “DZAM optimal $f_{s, \text{eff}}$,” is the DZAM-based adaptive $f_{s, \text{eff}}$ technique developed in this paper. For this case $f_{s, \text{eff}} \leftrightarrow (N_s, N_p)$ is provided by the efficiency maximizing curve of Fig. 15.

The results are shown in Figures 24-26 for output power 200W, 100W, and 50W, respectively. The shape of the three efficiency curves, which are similar at each power level, requires explanation. The fixed $f_{s, \text{eff}}$ curves experience a sharp drop in efficiency for values of $p$ within the dead zone, due to the doubling of switching loss imposed by the associated tri-interval operation. The exception to this is at $p = 0$, where the cessation of all switching produces the pass-through efficiency spike discussed in Section I and illustrated in Fig. 6.

The DZAM dual $f_{s, \text{eff}}$ curves consist of two portions. In the inner half of the dead zone, the technique alternates pass-through periods with tri-interval periods, with the former exactly canceling the doubling of switching loss produced by the latter. The combined result is a partial efficiency curve nearly equal to that which would occur with an imaginary fixed switching frequency converter which contained no dead zone. In the outer half of the dead zone, pass-through periods alternate with bi-interval periods, with the result that switching loss is one-half that of the fixed $f_{s, \text{eff}}$ system. This produces the sharp step up in efficiency seen at the dead zone boundary.

The DZAM optimal $f_{s, \text{eff}}$ curves generalize and extend the DZAM dual $f_{s, \text{eff}}$ curves by applying the optimal $f_{s, \text{eff}}$, and not just $\{f_{s, \text{nom}} f_{s, \text{nom}}/2\}$, as a function of $p$ and $I$. This results in very significant efficiency gains. In Fig. 24 (200W) the technique of this paper achieves a peak efficiency increase of 1.6% compared with fixed $f_{s, \text{eff}}$ and 0.8% compared with DZAM dual $f_{s, \text{eff}}$. As power drops to 100W in Fig. 25, fixed converter losses cause the efficiency to drop for all curves, but the peak efficiency improvements due to DZAM-based adaptive $f_{s, \text{eff}}$ increase to 2.1% (vs. fixed $f_{s, \text{eff}}$) and 1.0% (vs. DZAM dual $f_{s, \text{eff}}$). A further drop in power to 50W has a similar effect, with Fig. 26 exhibiting peak efficiency improvements of 3.2% vs. fixed $f_{s, \text{eff}}$ and 1.6% vs. DZAM dual $f_{s, \text{eff}}$. Across all three power levels these efficiency improvements reflect reductions in loss as high as 58%. Note that a closed loop system operating with steady state control jitter/wander will realize most of the peak efficiency gains of Figures 24-26, as the drop in efficiency just beyond pass-through has been transformed from a step to a smooth curve.

VI. CONCLUSION

A DZAM processor applies a nonlinear functional mapping to a NIBB converter duty cycle sequence in order to achieve specific system characteristics. In this paper a new DZAM nonlinearity is derived which produces a NIBB converter with an adaptive effective switching frequency, $f_{s, \text{eff}}$. This converter simplifies digital control through the use of a constant actual switching frequency $f_{s, \text{nom}}$, but nevertheless has average switching loss equal to that of a baseline converter with constant switching frequency equal to any specified value $f_{s, \text{eff}} \leq f_{s, \text{nom}}$. The DZAM-based adaptive $f_{s, \text{eff}}$ converter accomplishes this by interleaving pass-through with non-pass-through switching periods. As pass-through periods contain no switching, the amount of average switching loss can be controlled through specification of the total fraction of pass-through periods.

The DZAM nonlinearity derived here which accomplishes the interleaving also minimizes the DZAM error rms value, thereby reducing the increase in waveform ripple associated with a reduction in switching frequency. The degree to which the ripple increase is minimized is evaluated by comparing the DZAM-based inductor current waveform to that of the baseline non-DZAM fixed switching frequency converter. The results are summarized by two characteristics. First, for those $f_{s, \text{eff}}$ which divide $f_{s, \text{nom}}$, the $i_L(t)$ waveforms for the two systems are identical, meaning that the DZAM technique imparts the minimum possible increase in ripple. Secondly, for those $f_{s, \text{eff}}$ which do not divide $f_{s, \text{nom}}$, the additional increase in rms($i_L$) is limited to $<1\%$, but increases in peak($i_L$) as high as 24% are possible. However, these large peak increases only occur for specific windowing parameters, which will be avoided by algorithms or empirical procedures which set $f_{s, \text{eff}}$ for efficiency maximization.

The adaptation of switching frequency, either actual or effective, is necessary for the maximization of converter efficiency across the full range of conversion ratios and loads. The theory of this paper has been applied in the hardware and firmware development of a NIBB converter with DZAM-based adaptive effective switching frequency. Measured results indicate that unrealizable steady state operation at a pass-through efficiency spike is transformed into realizable operation near a pass-through efficiency maximum, with reductions in loss as high as 58% achieved.

VII. REFERENCES


