High Weighted Efficiency in Single-Phase Solar Inverters by a Variable-Frequency Peak Current Controller

Yoash Levron, *Member, IEEE*, and Robert W. Erickson, *Fellow, IEEE*

***Abstract*—This paper discusses a control method that achieves high weighted efficiency in solar microinverters. A challenge in microinverters is to achieve high efficiency over a range of output powers. To address this challenge, the proposed controller presents two primary benefits that enable such an efficiency profile, a switching frequency that scales with power, and a low peak current that enables efficient magnetic design of the inductor. At high powers, the switching frequency increases to minimize the root-mean-square (rms) current, and at low powers, the switching frequency decreases to minimize the switching loss. Since the peak inductor current is low, the inductor may be designed with fewer turns of wire, or with lower flux density, and is thus highly efficient. The proposed constant peak current switching scheme is implemented by a cycle-by-cycle predictive controller that uses a fast integrator to control the switching period, achieving high bandwidth and stability. This controller senses only the peak inductor current and, therefore, does not require expensive average current sensors. We demonstrate a low-cost inverter prototype with a 300-W solar panel. The prototype uses standard silicon devices and a small inductor of 360 μH to achieve a weighted efficiency of 99.15%.**

***Index Terms*—CEC efficiency, grid connected, inverter, micro inverter, photovoltaic, solar, weighted efficiency.**

I. Introduction

MICROINVERTERS are small single-phase power modules that connect directly to a photovoltaic (PV) panel and to the ac line [1]–[3]. Several advantages of these devices include individual maximum power point tracking of each PV panel, modular connection, and high reliability, because a system of microinverters has no single point of failure. Due to the varying nature of solar energy, microinverters are rated according to their weighted efficiencies. One example of a weighted efficiency standard is that published by the California Energy Commission [4], generally known as the CEC weighted efficiency. This standard uses a formula involving the inverter efficiencies at operating points ranging from 10% to 100% of the inverter rated power, where the 100% power point is assigned a small weighting factor of 5%, while intermediate power points are weighted more strongly. The purpose of these uneven weighting factors is to provide a better measure of the inverter performance with realistic variations of solar irradiance. Therefore, it is desirable to design inverters for high efficiency not simply at the full power operating point but instead over a range of powers such that the weighted efficiency is improved.

It is challenging to achieve high weighted efficiency with low-power microinverters, typically because these devices are required to be low cost. A study in [5], for example, shows that solar inverter efficiencies tend to decrease at low powers, with typical efficiencies in the range 91%–97% for inverters that are rated below 1 kW. However, recent studies have shown that efficiencies of microinverters can be improved, even in low-cost designs, by using better power stage topologies and better control methods [6], [7]. While high-power central inverters usually switch in continuous-conduction mode (CCM), with a small current ripple on the main inductor, microinverters usually operate either in discontinuous-conduction mode (DCM) or in boundary-conduction mode (BCM) [8]–[14]. This is primarily because the CCM method requires a large inductor and is hard switching, while DCM and BCM use smaller inductors and are soft switching. In [8], for example, the microinverter operates in DCM with a constant switching frequency, achieving a peak efficiency of 95.1%. Bo *et al*. [9] and Gonzalez *et al*. [11] demonstrate a modified buck topology that utilizes six switches and achieves a typical weighted efficiency of 96.5% and a peak efficiency of 97.4%. Amirahmadi *et al*. [12], [13] propose a BCM scheme that is zero-voltage switching and achieves peak efficiencies of 98.4% and 98.7%. Another study [14] uses BCM and CCM waveforms that has high current ripples to achieve a fully zero-voltage switching topology, a topology that enables peak efficiency of 97.5%.

Despite these recent advancements, the main barrier for higher efficiencies remains the switching loss. While the DCM and BCM control methods are soft switching, the frequency-dependent losses are still dominant in these approaches. One example is the loss due to the output capacitances of the switching devices, a loss mechanism that is voltage driven, does not scale with the output power, and hence, substantially degrades the inverter weighted efficiency. The popular BCM control scheme actually increases the switching frequency when the inverter output current is reduced, with corresponding penalty in the efficiency. Thus, to improve the weighted efficiency, it is desirable to lower the switching frequency at low output powers.

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Y. Levron is with the Electrical Engineering Faculty, Technion, Haifa 32000, Israel (e-mail: yoashl@ee.technion.ac.il).

R. W. Erickson is with the Department of Electrical, Computer, and Energy Engineering, University of Colorado Boulder, Boulder, CO 80309 USA (e-mail: rwe@colorado.edu).

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In the competitive business of solar grid-tied solar microinverters, cost and efficiency are critical. In a moderately shaded rooftop environment, distributed maximum power-point tracking (MPPT) can increase the annual energy capture by 5%–10% [15], and therefore, an increase in microinverter efficiency of even 1% or less can significantly impact the value proposition of grid-tied microinverter systems. We propose a new approach to microinverter design and control that can lead to significant improvements in efficiency and cost. This approach is based on a variable-frequency DCM approach that can reduce the inverter power stage average loss by a factor of two. The size and cost of the inverter inductors are significantly reduced, and the cost and complexity of current sensing are reduced as well.

We address this challenge by introducing a novel control scheme and an optimized magnetic design. The proposed research provides not only an improved peak efficiency but, more importantly, a substantially improvement in weighted CEC efficiency, which provides a competitive advantage and enables improved overall energy capture under varying irradiance conditions. The proposed design achieves this desired efficiency profile by small and low-cost components and a simple controller and, therefore, enables a substantial increase in average energy capture per invested capital and is highly competitive under the figure of merit of (watts-hour/$]. The controller operates in DCM with a constant peak current and scales the switching frequency as a function of the output power. At high powers, the inverter switches in BCM with low root-mean-square (RMS) current. At low powers, however, the switching frequency decreases and reduces the frequency-dependent losses. In addition, the constant peak current enables efficient design of the inductor. We also introduce a fast and stable cycle-by-cycle controller that does not require sensing of the average output current, thereby avoiding an expensive current sensor. Overall, the proposed method enables a low-cost design that operates with a small inductor and achieves a peak efficiency of 99.5% and a weighted efficiency of 99.15%.

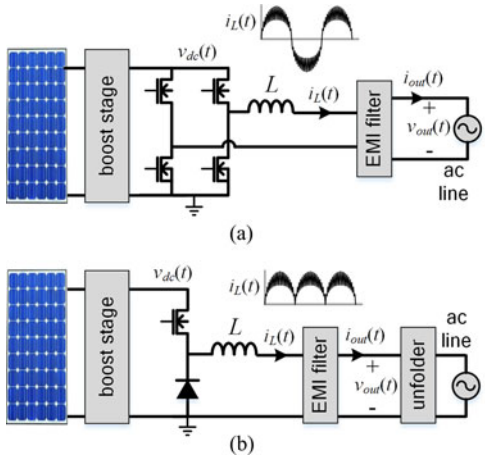

Fig. 1. Common microinverter power stages. (a) Full bridge. (b) Buck stage with an unfolder stage.

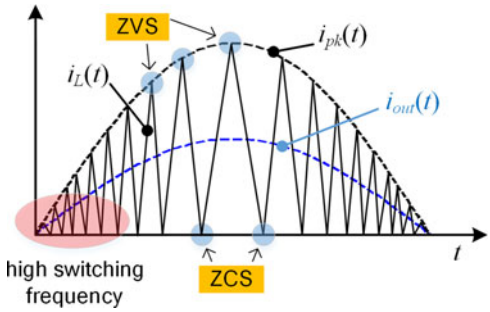

Fig. 2. Illustration of the inductor current in BCM, showing soft switching transitions (ZVS, ZCS) and the variations in switching frequency over the line cycle.

II. Variable-Frequency Peak Current Controller

In this section, we present the constant peak current switching scheme. This new scheme is derived through an analysis of weighted losses in BCM, an analysis that demonstrates that the dominant loss for BCM is switching loss. To improve the weighted efficiency, we explore which peak current is optimal at each output power and show that in DCM the optimal peak current is constant.

A common topology for microinverters is the two-stage topology [24], [25], which includes a boost stage and an inverter stage, as shown in Fig. 1. Typically, the boost stage tracks the maximum power point of the PV source and boosts the low PV input voltage to a higher voltage. The inverter stage generates the ac current that is injected to the ac line. Despite various new topologies that have been demonstrated in recent literature [5], the typical low-cost microinverter is still designed either as a full-bridge stage, or as a buck stage with an unfolder stage. The unfolder stage, if present, switches at the zero crossings of the line voltage to convert the rectified sinusoid at the buck output to a full sinusoid on the ac line.

An illustration of the BCM waveform is shown in Fig. 2. Although it is soft switching and operates with low rms current, a disadvantage of BCM is its high average switching frequency, which causes high switching losses. As demonstrated by (1), the BCM waveform has the highest switching frequency among all DCM waveforms. This is because the peak current of BCM is equal to $i_{pk}(t) = 2i_{\rm out}(t)$, which is the lowest possible peak current in DCM, and as a result, the switching frequency in BCM is maximal. Equation (1) also predicts that the switching frequency of BCM increases at low output powers, creating a switching frequency profile that causes disproportional switching losses at low powers. This is demonstrated by the last expression in (1) for which the power factor is unity and the switching frequency is proportional to $R_{\rm out}$. A lower output voltage $v_{\rm out}(t)$ results in a higher switching frequency, so the switching frequency and switching losses in BCM substantially increase at low voltages and low powers.

The switching frequencies in DCM and BCM are given by

$$\text{DCM}: \quad f_s(t) = \frac{v_{\rm out}(t)}{2L \cdot i_{\rm out}(t)} \left(1 - \frac{v_{\rm out}(t)}{v_{\rm dc}(t)}\right) \left(\frac{2i_{\rm out}(t)}{i_{pk}(t)}\right)^2$$

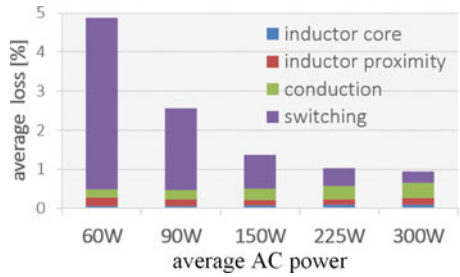

Fig. 3. Distribution of losses in BCM. The vertical bars represent average losses over an ac line cycle. The losses are shown in percent relative to the average ac output power. Switching losses dominate at low powers.

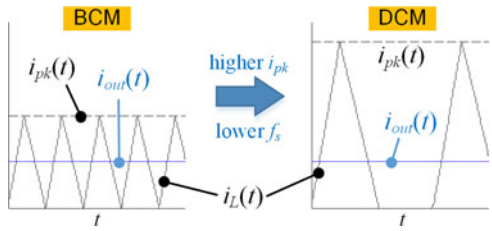

Fig. 4. By increasing the peak current in DCM, the switching frequency is reduced, while the average inductor current ($i_{\rm out}$) is unchanged.

$$\text{BCM}: \quad f_s(t) = \frac{v_{\rm out}(t)}{2L \cdot i_{\rm out}(t)} \left(1 - \frac{v_{\rm out}(t)}{v_{\rm dc}(t)}\right)$$

BCM with unity power factor

$$f_s(t) = \frac{R_{\rm out}}{2L}\left(1 - \frac{v_{\rm out}(t)}{v_{\rm dc}(t)}\right), \quad \text{where } R_{\rm out} = \frac{v_{\rm out}(t)}{i_{\rm out}(t)}. \quad (1)$$

Fig. 3 shows how the total loss in BCM distributes at various output powers. The losses in this figure are averaged over a line cycle and are shown in percent relative to the cycle-averaged output power. The total loss is composed of four types of loss: conduction losses, switching losses, proximity loss in the inductor, and core loss in the inductor. The losses are computed according to the calibrated loss model presented in Section IV. The conditions for the test are ac voltage of 220 $V_{\rm rms}$ @ 60 Hz, average ac power of 300 W, bus voltage of 425 V, and an inductor of 300 μH built on a PQ 26/20 core. The results demonstrate that the dominant loss mechanism in BCM at low powers is switching loss.

These data in Fig. 3 suggest that the weighted efficiency of BCM may be substantially improved if the low power switching losses are reduced. According to (1), this may be achieved by increasing the peak current. To demonstrate this idea, Fig. 4 compares a BCM waveform and a DCM waveform with a higher peak current. Although both waveforms provide the same average current ($i_{\rm out}$), the DCM waveform delivers more energy to the output at every cycle, and as a result, operates with a lower switching frequency that enables lower switching losses.

Thus, to achieve a certain average current, the controller can vary either the peak current or the switching frequency of the inductor current waveform. A higher peak current reduces the switching frequency but also raises the rms current and causes more conduction losses. At each operating point, there is an optimal peak current that minimizes the sum of these losses. To discover which peak current is optimal, Fig. 5 shows a plot of efficiency as a function of peak current (i_{pk}) at various dc operating points. Each curve in this figure corresponds to one dc operating point, with fixed average current and voltage ($i_{\rm out}$ and $v_{\rm out}$). The minimal i_{pk} at every curve is $2i_{\rm out}$, which corresponds to a BCM waveform. The dc operating points are selected with constant ratio of voltage and current $v_{\rm out}/i_{\rm out} = R_{\rm out}$ and, thus, reside on the same output sinusoid. The efficiency is computed according to the calibrated loss model presented in Section IV, with conditions as follows: $R_{\rm out} = 215.1W$, average ac power of 225 W, bus voltage of $v_{\rm bus} = 425$ V, and an inductor of 300 μH built on a PQ 26/20 core. Each curve is label by its output power $p_{\rm out} = v_{\rm out} i_{\rm out}$, which is given in percent relative to the maximal instantaneous output power of 450 W.

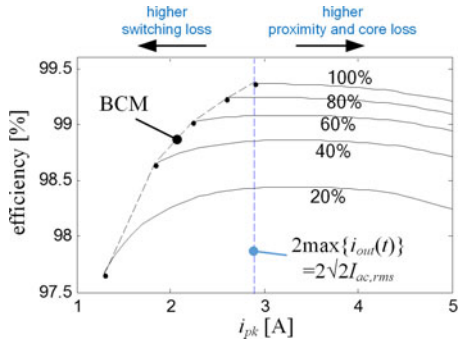

Fig. 5. Optimal peak current at various powers. Each curve shows the instantaneous efficiency as a function of peak current ($i_{\rm pk}$) at a certain dc operating point. The output power of each curve is shown in percentage relative to the peak instantaneous output power.

Fig. 5 reveals that the optimal peak current is nearly equal at all operating points and that this optimal value is $I_{pk} = 2\max\{i_{\rm out}(t)\}$, or $I_{pk} = 2\sqrt{2}I_{\rm ac,rms}$, where $I_{\rm ac,rms}$ is the rms current injected to the ac line. At peak currents that are lower than this optimal value, the frequency-dependent losses are dominant. However, at peak currents higher than this optimal peak value, proximity and core losses in the inductor dominate, because the inductor must support a higher peak current. This is because the minimal possible peak current of the inductor is the peak current that occurs at BCM at maximum power, which is $I_{pk} = 2\max\{i_{\rm out}(t)\}$. If the peak current is increased above this minimal value, the inductor must support a higher peak current and, therefore, must use more turns of wire or operate with a higher magnetic flux density, which results in increased proximity loss or core loss. Therefore, a peak current that equals to the peak current of BCM at full load, namely, $I_{pk} = 2\max\{i_{\rm out}(t)\}$, minimizes the sum of switching losses and the inductor-related losses and maximizes the efficiency.

A conclusion from Fig. 5 is that a controller that operates in DCM with a constant peak current of $I_{pk} = 2\sqrt{2}I_{\rm ac,rms}$ provides an optimized weighted efficiency in DCM. An illustration of the optimal inductor current over a line cycle is plotted at Fig. 6. The switching frequency of this waveform is given in (2) and plotted in Fig. 7. The controller scales the switching frequency according to the instantaneous output power. At low

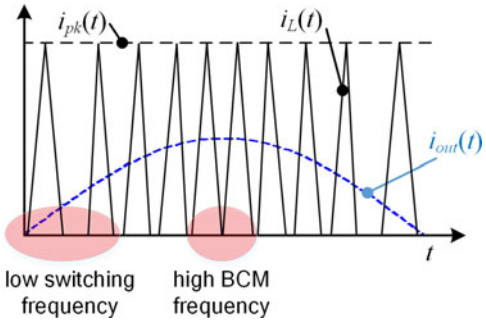

Fig. 6. Inductor current waveform of the proposed peak current controller. The inductor peak current is constant, and the switching frequency is scaled in proportion to the output current.

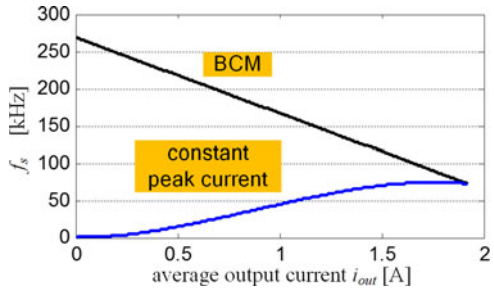

Fig. 7. Switching frequency of BCM and the proposed controller. Conditions: $L = 300\ \mu$H, $v_{\rm bus} = 425$ V, and $R_{\rm out} = 161.3\ \Omega$.

powers near the zero crossings, it operates with a low switching frequency. At high powers, the switching frequency increases and the controller operates at BCM. In addition, the inductor is designed with minimal peak current, and therefore, it uses the minimal number of turns and magnetic flux density. Combined, all these factors result in high efficiency at both low powers and high powers.

The switching frequency of the proposed constant peak current controller is

$$f_s(t) = \frac{2v_{\rm out}(t)i_{\rm out}(t)}{L \cdot I_{pk}^2}\left(1 - \frac{v_{\rm out}(t)}{v_{\rm dc}(t)}\right), \qquad (2)$$

$$\text{where } I_{pk} = 2\max_t\{i_{\rm out}(t)\} = 2\sqrt{2}I_{\rm ac,rms}.$$

III. Cycle-by-Cycle Controller

The previous section presented a switching scheme that operates in DCM with variable frequency and constant peak current and enables high weighted efficiency. In this section, we present a fast cycle-by-cycle controller that implements this desired switching scheme. A straightforward method for controlling the current is negative feedback. For example, the controller may sense the average output current $i_{\rm out}(t)$ and apply negative feedback to adjust the switching frequency $f_s(t)$ so that the output current is equal to a desired reference current. One disadvantage of this control method is that sensing the output current may prove challenging, especially in topologies where the output is floating, which typically requires expensive Hall-effect current sensors or current transformers in unique configurations. A second disadvantage of the negative feedback controller is that it is challenging to design a controller that achieves both high bandwidth and low harmonic distortion. The loop compensator must attenuate the switching frequency harmonics to avoid harmonic distortion in the output current. If this is accomplished by a slow lowpass filter, the open-loop bandwidth is reduced and the loop may present poor transient response and may even become unstable. Thus, the negative feedback compensator must take into account the contradicting constraints of bandwidth and harmonic distortion and, therefore, typically includes several poles and zeroes that increase its complexity.

In contrast, the control method we developed operates on a cycle-by-cycle basis and does not require sensing of the average output current. Instead of regulating the output current directly, the controller adjusts the net charge delivered by the inductor to the load at every cycle. At each cycle, the controller estimates the total charge of the inductor current and sets the switching period so that the average current for that period follows a current reference signal. The net charge is computed by the area of the inductor current waveform and is evaluated from the inductor peak current and total time in which the inductor conducts. The peak current is measured by a current sensing resistor to ground, and the total conduction time is measured by a voltage sensor that detects the voltage transient that occurs when the inductor current reaches zero. Thus, instead of using an expensive floating current sensor, the cycle-by-cycle controller uses only a simple analog circuit and two low-cost sensors. In addition, because the current is accurately controlled at each cycle, the bandwidth is high and the output current is generated with low harmonic distortion.

The analog circuit that implements the cycle-by-cycle controller is shown in Fig. 8. The control objective is to generate an inductor current with a constant peak current I_{pk} and an average current $i_{\rm out}$. Ideally, the average current follows a reference signal $i_{\rm ref}(t)$, so that $i_{\rm out}(t) = i_{\rm ref}(t)$, where $i_{\rm ref}(t)$ is a rectified sinusoidal signal synchronized to the ac line voltage. The main idea of this controller is instantaneously control the average current by adjusting the switching frequency. When a low average current is required, the switching frequency reduces and vice versa. The circuit shapes the desired current waveform by adjusting its on time ($T_{\rm on}$) and period ($T_{\rm s}$), and it does so by turning the FET on and off. The on time is controlled by a comparator that turns the FET off when the inductor current reaches the peak current (I_{pk}). The period is controlled by the FET turn-on transition and is adjusted so that the average current for the cycle is equal to the reference current $i_{\rm ref}$, as shown by the following equation:

$$i_{\rm ref} = \frac{Q}{T_s}, \quad Q = \frac{I_{pk}\left(T_{\rm on} + T_2\right)}{2} \quad \Rightarrow \quad T_s = \frac{Q}{i_{\rm ref}}$$
$$= \frac{I_{pk}\left(T_{\rm on} + T_2\right)}{2i_{\rm ref}} \qquad (3)$$

where Q defines the total charge or the area of the inductor current over one cycle.

The desired period time T_s presented in (3) is generated by an analog integrator, implemented by a capacitor ($C_{\rm int}$) and two current sources. The lower the $i_{\rm ref}$ is, the longer it takes

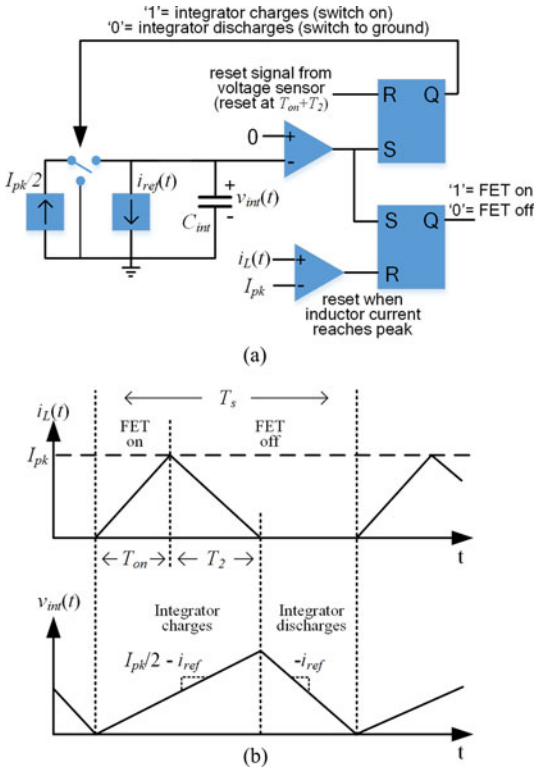

Fig. 8. Cycle-by-cycle controller. The peak inductor current is constant, and the cycle period T_s is adjusted to provide the desired average current. (a) Schematic circuit. (b) Typical inductor current and integrator voltage waveforms.

the capacitor $C_{\rm int}$ to charge and discharge, which lengthens the period T_s and reduces the average current. One current source constantly discharges the capacitor with a current $i_{\rm ref}$, and the other current source charges the capacitor with a current $I_{pk}/2$. This second source is controlled by a switch that enables or disables the charging current. A new cycle is initiated when the integrator voltage ($v_{\rm int}$) reaches zero. Two events are triggered at this point, the power stage FET is turned on, so the inductor current starts to increase, and the current source switch is closed, so the integrator starts to charge. The FET turns off when the inductor current (i_L) reaches the designated peak current (I_{pk}), but the integrator voltage starts to discharge only when the inductor current reaches zero again. At this moment, because no power device is conducting, the switching node voltage starts to oscillate between the input voltage and zero (see Section IV). This oscillation is detected by a voltage sensor that turns off the charging current source, and the integrator voltage ($v_{\rm int}$) starts to decrease. A new cycle is initiated only when the integrator voltage reaches zero again, so the positive change and the negative change in the integrator voltage during the cycle must be equal, as shown in the following equation:

$$\underbrace{\frac{(T_{\rm on}+T_2)\,(I_{pk}/2-i_{\rm ref})}{C_{\rm int}}}_{\text{positive change in integrator voltage}} = \underbrace{\frac{(T_s-T_{\rm on}-T_2)\,i_{\rm ref}}{C_{\rm int}}}_{\text{negative change in integrator voltage}}. \tag{4}$$

Fig. 9. Power stage of the inverter prototype.

By rearrangement of this equation, the resulting switching period T_s is found to be

$$T_s = \frac{I_{pk}\,(T_{\rm on}+T_2)}{2i_{\rm ref}}. \tag{5}$$

This is identical to the desired switching period presented in (3). Thus, by charging and discharging, the integration capacitor during the cycle, the switching period T_s is controlled as desired, without sensing the average current; so at every cycle, the average inductor current $i_{\rm out}$ is equal to the reference signal $i_{\rm ref}$.

IV. Experimentally Calibrated Loss Model and Optimal Design of the Inductor

In this section, we describe the loss model that was used to derive the results in Section II. The focus is on the switching loss mechanism, because of its complexity and dominance. We then use the loss model to explain further, why a constant peak current controller enables a highly efficient inductor design and how to optimize the inductor, in order to maximize the weighted efficiency of the inverter.

A. Experimentally Calibrated Loss Model

The loss model is designed to predict the power losses in a buck power stage that operates in DCM, with a lower FET and an upper diode, similar to the experimental power stage described in Section V. The power stage is shown in Fig. 9, and the switching devices, voltages, and other variables are detailed in Table I. The model parameters were calibrated using a least-squares criterion to a large amount of power loss data that were measured at various operating points and switching frequencies. As a result, the calibrated model predicts the power loss with a standard deviation error of 0.5 W, which translates to 0.16% error in efficiency at 300 W, so the model accurately predicts the loss in the experimental power stage.

The model includes four sources of loss: conduction losses, switching losses, inductor core loss, and inductor ac and dc copper losses. Conduction losses are computed by the following

TABLE I
PARAMETERS OF THE INVERTER PROTOTYPE

AC parameters	Peak ac power = 300 W, $V_{\rm ac} = 220 V_{\rm rms}$ @ 60 Hz $I_{\rm ac,rms}$ (max) = 1.36 A
Peak current	$I_{pk}\,(\max) = 3.9$ A
Input voltage	$V_{\rm dc}\,(\text{nominal}) = 425$ V
Switching devices	FET = FCD380N60E, Diode = RHRD660S9A FET gate driver = FAN3100TSX Current sense resistor $R_s = 50$ mΩ
EMI filter	$C_{\rm out} = 1.3$ μF (600 V), $L_{\rm EMI} = 500$ μH (2 A) each
Unfolder	4 BJT devices (FJP2145)
Main inductor	$L = 360$ μH, peak current = 4.3 A, $R_{\rm dc} = 110$ mΩ magnetic core PQ 26/20, 50-all ferrite, wire: Litz, 270 strands, #46, 36 turns, air gap = 0.24," auxiliary winding: 3 turns.

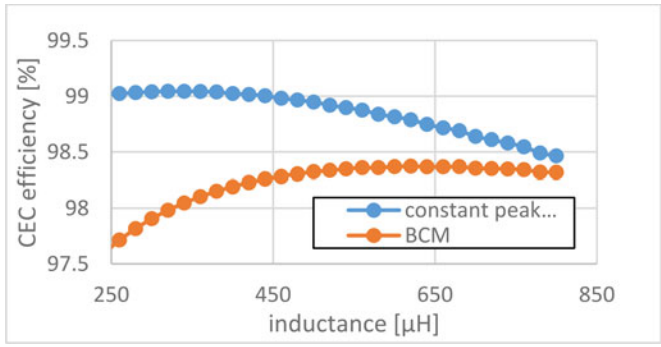

Fig. 10. Oscillations in the switching node voltage when the inductor current reaches zero in DCM. Ch2 (blue)—switching node voltage. Ch4 (green)—inductor current.

equation:

$$P_{\rm conduction} = \frac{R_{\rm FET,on}}{T_s}\int_0^{T_s} i_{\rm FET}^2\,(t)\,dt + \frac{1}{T_s}\int_0^{T_s} i_{\rm diode}\,(t)\cdot v_{\rm diode}\,(t)\,dt$$
$$R_{\rm FET,on} = 0.38\ \Omega, \quad v_{\rm diode} = 1.0466 + 0.118\cdot\ln\left(i_{\rm diode}\right) \tag{6}$$

where $i_{\rm FET}(t)$ and $i_{\rm diode}(t)$ are the current waveforms in the FET and diode during a cycle, T_s is the period of these waveforms, and $R_{\rm FET,on}$ is the FET on resistance. The diode forward drop $v_{\rm diode}$ depends on the diode current and is fitted to the experimental curve of the selected diode. These losses are computed per switching cycle and then averaged over a 60-Hz line cycle to predict the average loss.

The loss model also includes two loss mechanisms that are related to the inductor: core loss and proximity loss. Core losses are caused by ac variations in the magnetic flux density $B(t)$ within the magnetic core. AC and dc copper losses are Ohmic losses in the inductor wires that are increased through the skin and proximity effects. Both effects are well known. The core loss is evaluated by the iGSE model given in [26], and the proximity loss is evaluated by the model in [27]. To evaluate these losses, we used a computer program that fully modeled the inductor geometry, using parameters of the specific magnetic core, air gap, and Litz wire configuration. This program is available in [28].

Although DCM operation substantially reduces the diode reverse recovery loses, switching loss is nonetheless a dominant loss mechanism at high switching frequencies. A substantial loss mechanism is induced by semiconductor output capacitances and the associated ringing. An example of this well-known phenomenon is shown in Fig. 10. These oscillations cause energy losses that are manifested by a decay in the oscillations amplitude over time. In addition, when the FET is turned on, its parasitic drain-to-source capacitor is shorted and any energy stored in this capacitor is lost. The resulting loss depends on the exact amplitude of the oscillation when the FET turns on. If most of the oscillating energy is stored in the inductor during the turn on, the parasitic capacitor voltage is low and the energy loss is low. However, if most of the oscillating energy is stored in the parasitic drain–source capacitor, the energy loss is high.

Predicting the exact ringing loss in every dc operating point is very challenging, because this loss highly depends on the moment of switching and, thus, is largely affected by small parasitic components. The main problem is that the amplitude of the oscillating voltage at the moment of switching is unknown, and therefore, the energy stored in the drain–source capacitance is also unknown. However, over an ac line cycle, the operating point varies, and the switching occurs at many different voltages, and as a result, the average loss over a cycle is well predicted by a probabilistic model, which assumes that the oscillating voltage distributes randomly over a range. Such a model is derived next.

At each time point, the voltage range in which the switching node oscillates is defined by $\{v_{\rm low}(t), v_{\rm high}(t)\}$, where $v_{\rm low}(t)$ is the low bound of the oscillating voltage and $v_{\rm high}(t)$ is the high bound of the oscillating voltage. Time $t = 0$ is the moment in which the inductor current reaches zero and the oscillations commence. At this initial time, the voltage oscillates between the input voltage $V_{\rm dc}$ and the voltage $V_{\rm dc} - 2v_{\rm out}$. After infinite time, if no switching occurs, all the energy is lost and the switching node voltage is constant at $V_{\rm dc} - v_{\rm out}$. Between these points, the range of oscillations decays exponentially, at a rate proportional to the inductance L, as described by the following equation:

$$\begin{aligned} v_{\rm high}(0) &= V_{\rm dc}, \qquad v_{\rm low}(0) = V_{\rm dc} - 2v_{\rm out} \\ v_{\rm high}(\infty) &= V_{\rm dc} - v_{\rm out}, \qquad v_{\rm low}(\infty) = V_{\rm dc} - v_{\rm out} \\ &\Downarrow \\ v_{\rm high}(t) &= V_{\rm dc} + v_{\rm out}\left(-1 + \exp\left(-\frac{R_d t}{2L}\right)\right) \\ v_{\rm low}(t) &= V_{\rm dc} + v_{\rm out}\left(-1 - \exp\left(-\frac{R_d t}{2L}\right)\right) \end{aligned} \tag{7}$$

where R_d is a parameter that governs the rate of decay in the oscillating voltage amplitude. The value used in the calibrated model is $R_d = 11\ \Omega$.

The switching loss due to ringing is evaluated by the function $E_{\rm oss}(v_{ds})$, which defines the energy stored in the FET drain–source capacitance as a function of drain–source voltage. This function may be found in the FET datasheet (see Table I). The loss due to the decay in the oscillation amplitude over time is defined as $P_{\rm ringing\text{-}resistive}$ and is calculated by the difference of the initial energy in the drain–source capacitor $E_{\rm oss}(V_{\rm dc})$ and the maximal energy in this capacitor at the time of the switch $E_{\rm oss}(v_{\rm high})$. The second loss component describes the loss of energy when the drain–source capacitance is shorted and is defined as $P_{\rm ringing\text{-}capacitive}$. This loss is computed by the average energy loss over the range $v_{\rm low}$ and $v_{\rm high}$. The total switching loss is evaluated by the following equation:

$$\begin{aligned} P_{\rm switching} &= P_{\rm ringing\text{-}resistive} + P_{\rm ringing\text{-}capacitive} \\ P_{\rm ringing\text{-}resistive} &= f_s \cdot \left(E_{\rm oss}\left(V_{\rm dc}\right) - E_{\rm oss}\left(v_{\rm high}\right)\right) \\ P_{\rm ringing\text{-}capacitive} &= f_s \cdot \frac{1}{v_{\rm high} - v_{\rm low}} \int_{v_{\rm low}}^{v_{\rm high}} E_{\rm oss}\left(v\right) dv. \quad (8) \end{aligned}$$

B. Optimal Design of the Inductor

It is a common practice to design an inductor that maximizes the efficiency at one power level, usually the peak power. By contrast, in this study, the inductor is designed to maximize the weighted efficiency. For a given wire and magnetic core geometry, the design of the inductor is governed by two free parameters, the maximum amplitude of the magnetic flux density $\Delta B_{\rm max}$ and the inductance L. Other parameters involved in the inductor design such as the number of turns and the air gap are determined by these two free parameters. Therefore, the challenge when designing the inductor is to choose the magnetic flux density $\Delta B_{\rm max}$ and inductance L such that the weighted efficiency is maximized.

The tradeoff in the choice of the inductance L is between Ohmic losses (conduction + proximity) and frequency-dependent losses (switching + core + proximity). This is because a higher value of inductance L results in lower rms inductor currents but requires higher switching frequencies. Likewise, the tradeoff in the choice of $\Delta B_{\rm max}$ is between core loss and proximity loss. When $\Delta B_{\rm max}$ is low, the core loss decreases but more turns of wire must be used, so the Ohmic proximity losses increase. The opposite occurs when $\Delta B_{\rm max}$ is high. In addition, the inductor air gap must be sufficient to prevent saturation of the required peak current I_{pk}. With higher peak currents, a longer air gap is required to support the same $\Delta B_{\rm max}$, and as a result, more turns of wire must be used. Thus, to maximize the weighted efficiency, the inductor peak current must be minimized. This is why the proposed constant peak current controller uses the lowest possible peak current in DCM.

To find the optimal values of the inductance L and magnetic flux density $\Delta B_{\rm max}$, we used a computer program that numerically scanned the weighted efficiency of every combination of these two parameters. The program runs over each output power level and over single dc operating points in the output sinusoid and computes the efficiency at each operating point, using the calibrated loss model. The resulting efficiency data is averaged according to the CEC efficiency formula (see Section V). Typical results of this simulation are shown in Fig. 11, for a PQ 26/20 magnetic core, and conditions as detailed in Table I.

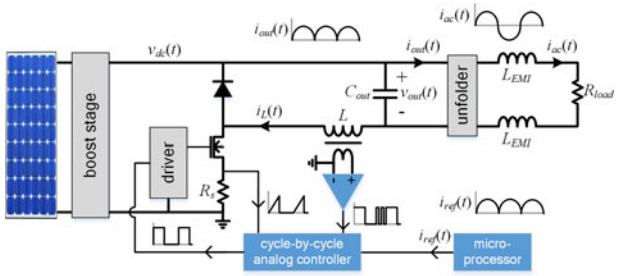

Fig. 11. Weighted CEC efficiency with a PQ 26/20 magnetic core, for a BCM controller and the proposed constant peak current controller.

Fig. 11 shows the optimal inductance values (L) for the BCM control method and for the proposed constant peak current method. These optimal inductance values achieve the best mix of frequency-dependent losses and Ohmic losses. Notice that a higher inductance value in Fig. 11 does not mean a larger inductor, because the magnetic core is the same (PQ26/20) at all the data points. Nevertheless, the optimal inductance value in BCM is considerably higher in comparison to the optimal value of the constant current controller. The reason for this difference is that a higher inductance is needed in BCM, to reduce the otherwise high switching frequencies that occur with this control method. The higher inductance requires more turns of wire on the inductor core, which is one reason why BCM is less efficient in comparison to the proposed constant peak current controller.

V. Experimental Microinverter Prototype

The proposed controller was tested on a microinverter prototype, whose power stage is shown in Fig. 8. The prototype is designed for a PV panel with a peak power of 300 W and interfaces an output voltage of $220\mathrm{V_{rms}}$ at 60 Hz. The design parameters are detailed in Table I.

The inverter stage consists of a buck stage and an unfolder circuit. The buck stage is constructed with an "upside-down" configuration, using a low-side FET, and an upper diode, a configuration that enables to drive the FET with an inexpensive low-side gate driver. The unfolder circuit controls the polarity of the current and converts the rectified sine wave at the output of the buck stage to a full sine wave at the ac line. This circuit is implemented by four BJT devices, arranged in a full-bridge topology, which changes polarity when the ac line voltage crosses zero. Since the BJTs are switched only twice per line cycle, switching losses in the unfolder are low, so this circuit is highly efficient.

A short overview of the entire control system is shown in Fig. 12. A primary function of the step-up stage is to boost the voltage efficiently. To implement an efficient power stage, the step up stage is designed as a "dc transformer" (DCX),

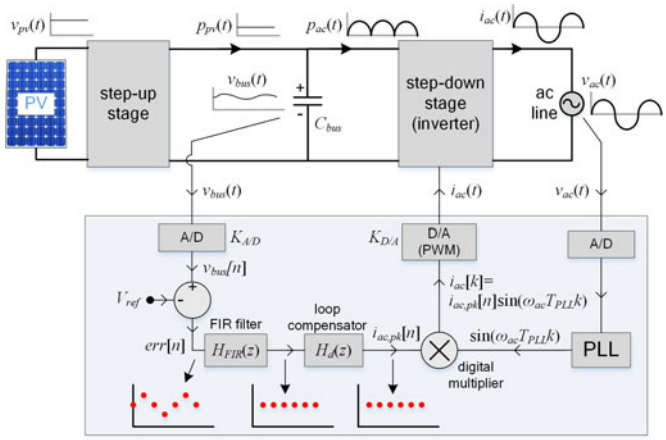

Fig. 12. System controller that regulates the voltage on the bus capacitor. The FIR filter removes the second harmonic ripple, providing a clean feedback signal that drives the output current with high bandwidth and zero distortion.

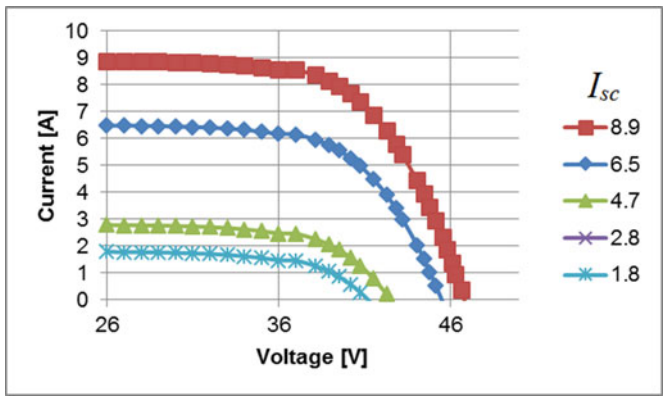

Fig. 13. Curves of the 300 W PV panel used in the experiment, given for different short-circuit currents ($I_{\rm sc}$).

Fig. 14. Inverter waveforms at a dc operating point. Ch1 (yellow) cycle-by-cycle integration capacitor voltage $v_{\rm int}(t)$, Ch2 (blue) auxiliary winding voltage sensor, at comparator output, Ch4 (green) inductor current $i_L(t)$. Conditions: $V_{\rm dc} = 426.8$ V, $I_{\rm dc} = 0.98$ A, $v_{\rm out} = 330.1$ V, and $i_{\rm out} = 1.259$ A.

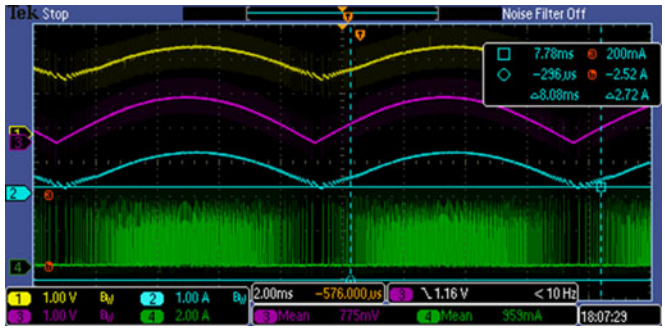

Fig. 15. Inverter waveforms over a line cycle, showing the output current and output voltage. Ch1 (yellow) ac line voltage sensor, Ch2 (blue) ac current $i_{\rm ac}(t)$, Ch3 (magenta) reference signal $i_{\rm ref}(t)$, Ch4 (green) inductor current $i_L(t)$. Conditions: $V_{\rm dc} = 425$ V, $I_{\rm dc} = 0.462$ A, and $R_{\rm load} = 253\ \Omega$

which is highly efficient. The proposed controller uses a digital finite impulse response (FIR) filter that samples the bus voltage at a slow sampling rate, which is a multiple of the ac line second harmonic frequency. This digital filter extracts the low-frequency components of the bus voltage signal, measuring the average bus voltage, while effectively filtering the noise of the second harmonic ripple. The digital filter thus combines three properties that are desired in this application: it operates at a very low sampling frequency and is low cost; it attenuates the second-harmonic ripple well and eliminates the distortion due to a notch in its transfer function; and it is quick enough to obtain highly stable dynamic response that maintains the bus voltage well regulated during transients.

The inverter power stage is controller the analog cycle-by-cycle circuit presented in Fig. 8, using the integration capacitor to control the cycle time T_s. The circuit generates a rectified output current $i_{\rm out}(t)$ that follows a reference signal $i_{\rm ref}(t)$, generated by a microcontroller. The peak current of the inductor waveform is constant at all operating points, except near the ac voltage zero crossings, where the peak current is decreased to reduce the crossover distortion. The hardware implementation is similar to the schematic circuit shown in Fig. 8, where the current sources are implemented with closed-loop operational amplifiers. The control circuit uses two sensors—a current sense resistor R_s and a voltage sensor—on the inductor. The current sense resistor is located between the FET source and ground and senses the rising slope of the inductor current. The only function of this sensed signal is to turn off the FET when the inductor current reaches the designated peak current I_{pk}. The voltage sensor is implemented by a comparator that connects to an auxiliary winding (three turns) on the inductor. Its purpose is to detect the moment in which the inductor current reaches zero, the moment in which the cycle-by-cycle integrator voltage starts to discharge (see Fig. 8). As explained in Section IV, at this moment, the switching node voltage starts oscillating and the voltage across the inductor changes polarity. This change is detected by the comparator, which resets the controller SR flip–flop (see Fig. 13). The oscillating output of the auxiliary winding comparator is shown in Fig. 14 (blue waveform). This graph also shows the voltage across the cycle-by-cycle integration capacitor ($v_{\rm int}$, yellow waveform). The inverter waveforms over a 60 Hz line cycle are shown in Fig. 15.

The efficiency of the inverter is measured at static dc operating points. These tests are done with a power supply at the input and a variable-load resistor ($R_{\rm load}$) at the output. To increase the accuracy of the measurements, the meters at the input and output

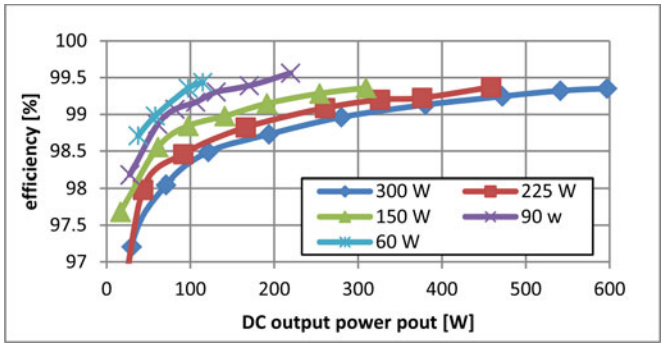

Fig. 16. Efficiency measurements at dc operating points, for various average ac powers.

TABLE II
CEC EFFICIENCY

CEC Power Level	Weight	Average AC Power $P_{\rm ac}$	Average Loss Over AC Cycle	Average AC Efficiency
100%	0.05	300 W	2.6 W	99.13%
75%	0.53	225 W	1.97 W	99.12%
50%	0.21	150 W	1.26 W	99.16%
30%	0.12	90 W	0.7 W	99.22%
20%	0.05	60 W	0.45 W	99.24%
10%	0.04	30 W	0.24 W	99.2%
Overall Weighted CEC Efficiency = 99.15%				

are filtered by large EMI inductors. The efficiency results are shown in Fig. 16. The various curves in the figure correspond to tests with different average ac powers ($P_{\rm ac}$). At each such test, the load resistor is set to $R_{\rm load} = V_{\rm ac,rms}^2/P_{\rm ac}$ and the instantaneous output power is scanned in the range $0 \ldots 2P_{\rm ac}$.

At each power level, the ac efficiency is computed by averaging the dc efficiencies over a line cycle. The results are again averaged by the CEC weighted average formula to obtain the overall CEC efficiency. The ac efficiency is computed by (9), and the results are summarized in Table II

$$\text{AC efficiency } \eta_{\rm ac} = \frac{\int_0^{\pi/\omega {\rm ac}} p_{\rm out}\,(t)\,dt}{\int_0^{\pi/\omega {\rm ac}} \left(p_{\rm out}\,(t)\,/\eta_{\rm dc}\,(p_{\rm out}\,(t))\right)dt},$$
$$\text{where } p_{\rm out}\,(t) \;=\; P_{\rm ac}\sin^2\left(\omega_{\rm ac} t\right). \tag{9}$$

In this equation, $P_{\rm ac}$ is the average ac power, $p_{\rm out}(t)$ is the output power at a dc operating point, and $\eta_{\rm dc}(p_{\rm out})$ is the efficiency at those operating points, as shown in Fig. 16. The weighted CEC efficiency is found to be 99.15%.

Table II shows that the efficiency is almost constant at all power levels. This flat efficiency in the curve is a key advantage of the proposed approach and is made possible by the innovative magnetic design and control method that is introduced in this work, especially by the low magnetic saturation current and variable switching frequency. Instead of maximizing the efficiency at a single point, as done in prior studies, our study targets high efficiency at all power levels, and a proof that this method is successful is given in Table II, which shows that the efficiency is indeed constant. This result is what enables high weighted efficiency and high overall energy capture.

VI. CONCLUSION

This study presents a switching scheme and a control method that achieve high weighted efficiency in solar microinverters. Through a detailed analysis of the losses in DCM, we explore what is the best balance between switching frequency and peak current at various powers. The conclusion is that the sum of conduction losses and frequency-dependent losses is minimized by a peak current that is constant at all output powers, and therefore, a switching scheme that uses variable frequency and constant peak current optimizes the weighted efficiency. This scheme presents two main benefits, a switching frequency that scales with power and a low peak current that enables efficient magnetic design of the inductor. At high powers, the switching frequency matches the frequency of BCM, so the rms current is low, and at low powers, the switching frequency decreases and the switching losses are low. Since the peak inductor current is constant and low, the inductor may be designed with fewer turns of wire, or with lower flux density, and is thus highly efficient, even when implemented on a small magnetic core. The proposed constant current switching scheme is controlled by a cycle-by-cycle controller that utilizes a fast integrator to set the period time, achieving high bandwidth and good stability. This controller only senses the peak inductor current, and so does not require expensive current sensors. We demonstrate a low-cost design that uses standard silicon devices and a small inductor of 360 μH and achieves a weighted efficiency of 99.15%.

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Yoash Levron (M'14) received the M.Sc. and Ph.D. degrees in electrical engineering from the University of Tel-Aviv, Tel-Aviv, Israel, in 2007 and 2012, respectively.

Since 2014, he has been an Assistant Professor with the Electrical Engineering Faculty, Technion, Haifa, Israel. His current research interests include sensing and estimation in power networks, control of distributed generation units and energy storage devices, signal processing and pattern recognition in power systems, and power conversion for photovoltaics and fuel cells.

Robert W. Erickson (S'82–M'82–SM'97–F'01) received the B.S., M.S., and Ph.D. degrees from the California Institute of Technology, Pasadena, CA, USA, in 1978, 1980, 1982, respectively.

Since 1982, he has been with the Faculty of the ECEE Department, University of Colorado Boulder, USA, where he was the Chair in 2002–2006 and 2014–2015. He and Prof. Maksimovic codirect the Colorado Power Electronics Center. He is an author of the textbook *Fundamentals of Power Electronics*. His current research interests include electric vehicle power electronics (charger and drive train power conversion), grid interface of solar and wind power systems, low-harmonic rectification, resonant power conversion, and power electronics modeling and control.

Dr. Erickson a Fellow of the UC-B/NREL Renewable and Sustainable Energy Institute.