A Microinverter for Building-Integrated Photovoltaics

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Abstract—A transformerless microinverter is described that is intended for integration into building materials such as residential roof shingles. The inverter achieves low profile (3 mm), high efficiency (95.1%) and high-reliability capacitive energy storage using 125˚C ceramics. It is intended to interface a 25 W photovoltaic array such as a small thin-film residential roof shingle to the 120 V ac utility. Design tradeoffs involving cost and efficiency are described, and operation of an experimental prototype is documented.

I. INTRODUCTION

Development of new technologies for low-cost manufacturing of thin-film photovoltaic (PV) power cells will enable new types of building materials that integrate photovoltaic power generating elements. In this role, the photovoltaic modules become architectural elements, requiring properties such as a low profile, ease of connection to the utility system, and the ability to maximize energy capture in a complex physical environment having shadows and reflections. An example is the residential roof shingle, where the photovoltaic modules have the appearance of asphalt shingles. To maximize energy capture on a complex multifaceted roof, localized smart controllers are required that can track the PV peak power points on a fine scale. In addition, the ability to generate ac simplifies connection to the ac utility system and can substantially reduce installation and other balance-of-system costs. Meeting these requirements requires low-power inverters having very low profile and high efficiency. There is extensive literature on PV inverters and microinverters, several of which are listed here [1-9]. However, there is no current solution that can meet the requirements above, and hence a new inverter approach is needed.

A. Goals and Requirements

A typical residential roof shingle might have 0.25 m² of active PV area. At a solar irradiance of 1000 W/m² and with an assumed efficiency of 10%, the solar array would produce 25 W. Hence, a rated inverter power of 25-30 W is desired. The conclusions of this paper can be extended to somewhat higher power levels (~100 W) if desired, although the inductor profile will be increased. Thin film PV cells are easily cut and interconnected to form high-voltage arrays; it is assumed here that this technology is employed to generate the approximately 200 V dc required to drive a 60 Hz 120 V ac inverter. Alternately, a dc–dc converter could be added to boost the PV panel voltage to the required level. To fit inside a laminated roof shingle, the inverter must have an extremely low profile,
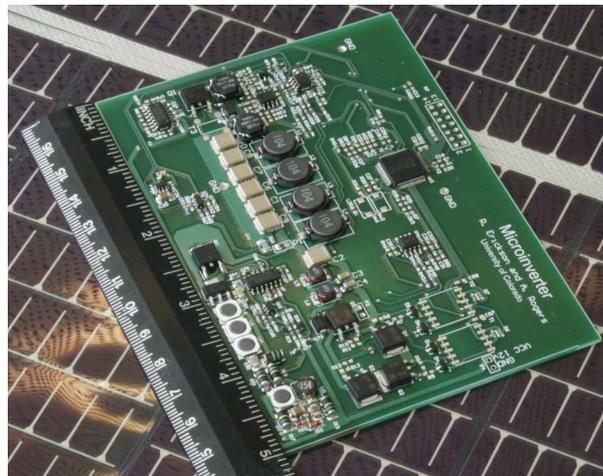

Figure 1. BIPV microinverter prototype, having a power component height of 3 mm, a PCB area of 3" x 5", and employing 125˚C components

such as 3 mm. Additionally, the inverter components must operate in the high temperatures encountered on the roof.

This paper describes a prototype integrated photovoltaic power module, intended to meet the needs of grid-tied building-integrated photovoltaic (BIPV) systems. Benefits of the proposed approach include:

- Low profile (3 mm) allows in-laminate operation and integration into roofing material
- High efficiency (95.1% predicted worst case)
- High reliability capacitive energy storage (125˚C ceramic capacitors)
- Low cost of power stage (< 25¢/W_{pk}) and reduced installation cost
- High quality ac line current waveforms meet the IEEE 1547 limit of THD < 5% as well as FCC conducted EMI requirements

The current cost of photovoltaic panels is approximately $4 per peak watt ($W_{pk}$). The balance-of-system (BOS) costs are approximately $4 to $6 per peak watt, and include the costs of engineering, installation, wiring, switchgear, and inverters. Inverter retail cost is approximately $0.80/$W_{pk}$. The US Department of Energy goals [10] include reduction of the total system cost to $3.25/$W_{pk}$ by 2015. Integration of the system elements—PV materials, power electronics, and interconnections—into building materials that are easily and quickly installed is a key strategy in the reduction of BOS cost. Because of the relatively low cost of power electronics, there are opportunities and needs for employment of power electronics to reduce the overall BOS cost through this system integration.
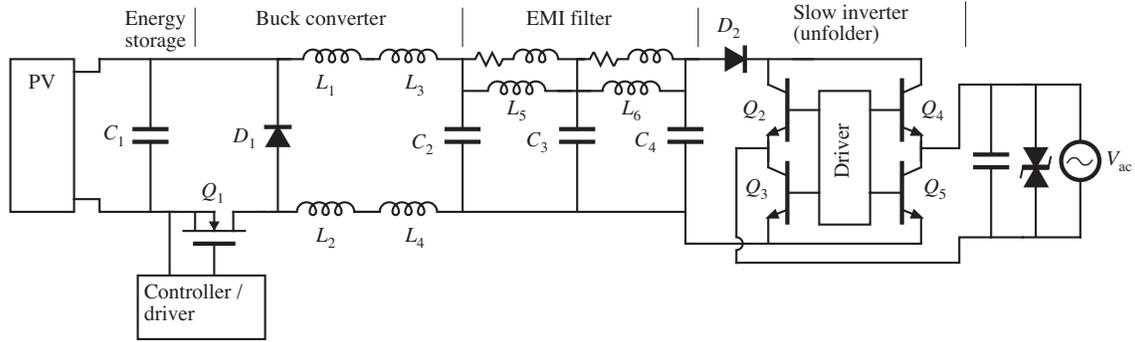
Figure 2. Power stage schematic

B. Outline of Discussion

The key features of the proposed inverter system are described in Section II. The primary challenges are the achievement of very high efficiency and very small inductor size. The use of discontinuous conduction mode (DCM) or boundary conduction mode (BCM) are found to be effective solutions, because these approaches employ relatively low inductance and also eliminate the switching loss induced by diode reverse recovery. High-voltage 125°C X7R ceramic chip capacitors are used as the 120 Hz energy-storage element; these are the most expensive part of the inverter, but at $0.09/W$_{pk}$ they are substantially less expensive than the PV array.

The hybrid analog-digital control system is described in Section III. Average current-mode control is employed to achieve high-quality ac line current waveforms. A small digital controller performs the other required grid-interface functions, such as ac line synchronization and anti-islanding.

A detailed inverter model was developed, and is described in Section IV. The use of this model was key in finding an approach that could meet the efficiency, low profile, and high temperature requirements of this application. Experimental measurements confirmed the accuracy of the loss model.

Operation of an experimental prototype is documented in Section V. This prototype employs low-profile high-temperature components, achieves high-quality ac line current waveforms with high efficiency, and demonstrates the feasibility of the proposed approach. Conclusions are summarized in Section VI.

II. HIGH-EFFICIENCY LOW PROFILE APPROACH

The major power stage elements are illustrated in Fig. 1. The photovoltaic array supplies a dc input of approximately 200 V to the inverter. This relatively high voltage can be produced directly by a series-connected thin-film PV array, or alternatively a lower-voltage PV string may be interfaced through a dc-dc converter. An energy storage capacitor C_1 is connected across the panel output; this capacitor is required to store and supply the difference between the constant power of the PV array and the twice-line-frequency power variations of the single-phase inverter. A dc–dc buck converter synthesizes a rectified sine wave and performs all control functions. This buck converter operates in the discontinuous conduction mode, and employs a single high-voltage MOSFET with low-side driver. A dc-side EMI filter reduces conducted emissions to meet FCC standards. A slow inverter switches at the ac line frequency, using inexpensive bipolar junction transistors (BJTs). A similar approach employing a high-frequency isolated dc–dc bridge followed by an unfolder was employed in [3,4]. The key difference in the system proposed here is the use of discontinuous conduction mode (DCM) or boundary conduction mode (BCM) to achieve a very low profile with high efficiency. Each of these elements is discussed in detail below.

A. Continuous vs. Discontinuous/Boundary Conduction Mode

Several power stage approaches were considered, and their performances were modeled using a detailed simulation. Details of the simulation model and key assumptions are documented in Section IV. The model was validated with a dc experiment, as noted in Section V. Designs having small inductor current ripple (continuous conduction mode, or CCM) as well as large inductor current ripple (discontinuous conduction mode, or DCM), were considered, and this was found to be the dominant factor in the choice of approach.

Operation of the inverter in CCM was judged unsuitable for this application because of the switching loss induced by diode reverse recovery. Use of a switching frequency of 130 kHz with commercial ultrafast rectifiers and 4 mH of inductance would lead to a predicted switching loss of

TABLE I
PREDICTED LOSS BUDGET, CCM

Switching loss	1.319 W
MOSFET and diode conduction loss	0.316 W
Inductor losses	0.297 W
Capacitor ESR loss	0.009 W
Unfolder conduction loss	0.075 W
Unfolder driver power consumption	0.154 W
MOSFET driver power consumption	0.076 W
Controller power budget	0.050 W
Total loss	2.295 W
Predicted efficiency, rated power	91.6%

Switching loss	0.113 W
MOSFET and diode conduction loss	0.349 W
Inductor losses	0.251 W
Capacitor ESR loss	0.154 W
Unfolder conduction loss	0.075 W
Unfolder driver power consumption	0.154 W
MOSFET driver power consumption	0.076 W
Controller power budget	0.050 W
Total loss	1.279 W
Predicted efficiency, rated power	95.1%

approximately 1.3 W, a total estimated loss of 2.3 W, and an efficiency of 91.6% as listed in Table I. CCM inductors meeting the 3 mm height constraint are not available, and 6 mm CCM inductors having a total inductance of 3.76 mH and a total resistance of 5.48 Ω instead would be required. The predicted efficiency was judged unacceptable. Although the switching loss could be reduced by lowering the switching frequency, this would further increase the inductor size.

A solution is the use of large inductor current ripple, in the discontinuous or boundary conduction mode. This approach was found to reduce both switching loss and inductance value by a factor of ten. With a fixed switching frequency of 130 kHz, this approach requires approximately 400 μH of inductance, and leads to a predicted switching loss of 0.11 W. Suitable 100 μH drum cores having a 3 mm height are available. Four of these (L_1 to L_4) were connected in series to obtain 400 μH.

The predicted losses for the DCM design are listed in Table II. Although the semiconductor conduction losses and the capacitor equivalent series resistance (ESR) losses are increased, the substantial decrease in switching loss more than compensates. Further, the inductor loss is slightly decreased because the smaller inductance allows a commensurately smaller resistance. The reduced switching loss of 0.11 W leads to a total predicted loss of 1.28 W and an efficiency of 95.1% at rated load. Similar results can be obtained in the variable-frequency boundary conduction mode.

B. Power Stage Topology
Either the conventional H-bridge circuit or the buck-plus-unfolder approach [3,4] can operate in DCM. However, operation in DCM requires a substantial differential-mode filter to attenuate conducted EMI to meet regulatory limits. The H-bridge approach requires that this filter be placed on the ac side and hence employ expensive ac-rated capacitors having a high profile. The buck-plus-unfolder approach can employ low-profile dc-rated capacitors by positioning the EMI filter on the dc side of the unfolder, and by avoiding high-frequency switching of the unfolder elements. Hence, the power stage configuration of Fig. 2 is selected.

The unfolder block is a slow inverter, whose transistors switch at the zero crossings of the ac line voltage waveform.
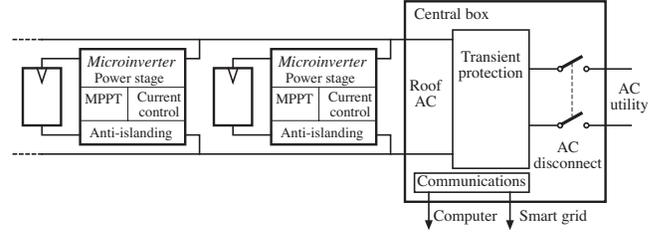

Figure 3. PV rooftop system consists of parallel-connected microinverters, plus a central box that includes ac transient protection, ac disconnect, and communications to smart grid and/or user computer interface.

This switching is controlled by the buck converter controller, providing a degree of immunity from noise in the ac line voltage. Figure 1 illustrates one possible realization of the unfolder, using diode D_2 and bipolar junction transistors (BJTs) Q_2 through Q_5. Diode D_2 protects the dc-side elements of the system from utility voltage transients, and prevents inrush currents.

A small low-profile transient protector is included on the ac side of the unfolder. The primary system transient protection is located in a central box as illustrated in Fig. 3. This removes the low-profile requirement from the transient protector, with substantial cost benefits. The central transient protection can be designed using methods such as in [18]. The central box may also include an ac disconnect switch, as well as smart grid and/or user interfaces.

C. Energy Storage Capacitor
An energy storage element, required for maximization of energy capture in single-phase systems, is connected across the terminals of the photovoltaic array. Conventional inverters employ electrolytic capacitors for this purpose; however, such capacitors do not exhibit the very low profile required for integration into a thin film module, nor do they meet the requirements of long life and high temperature operation. Hence, high voltage ceramic chip capacitors (X7R) are employed. Such capacitors exhibit low profiles of less than 3 mm and are capable of high temperature operation. Figure 4 illustrates the cost per PV W_{pk}, based on published domestic prices in quantities of several thousand. It can be seen that there is a substantial advantage to performing the energy storage function at high voltage. While these capacitors are the most expensive element within the system, their price may be
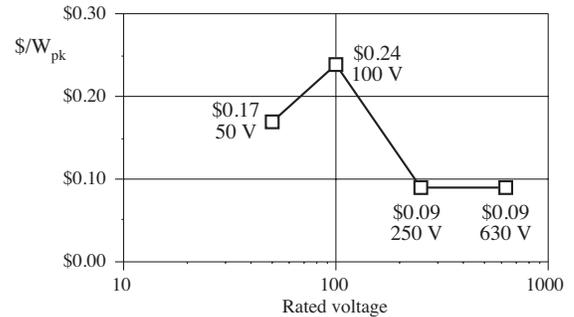

Figure 4. Specific cost (dollars per rated PV watt) of X7R energy storage capacitors, domestic sources
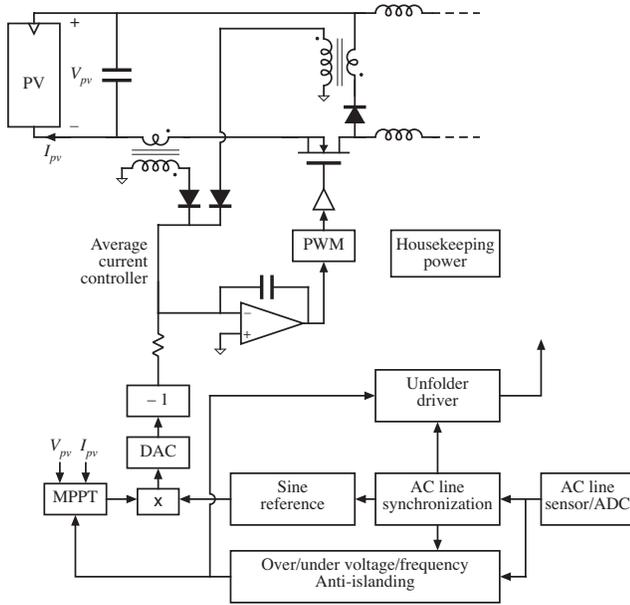
Figure 5. Major elements of control system

justified by their increased life, their very low profile that enables integration into the roofing laminate, and the potentially reduced cost of installation afforded by the distributed microinverter approach.

III. CONTROL SYSTEM

A block diagram of key controller elements is illustrated in Fig. 5.

Average current-mode control [11] is employed to cause the average DCM inductor current to follow a reference signal generated by a digital-to-analog converter (DAC). Small current-sense transformers produce currents proportional to the buck MOSFET and diode currents; the sum of these currents is proportional to the inductor current. The DAC reference is subtracted from the sum of these currents, and the result is fed into an op-amp integrator circuit whose output drives a pulse-width modulator (PWM) and the MOSFET. This circuit varies the MOSFET duty cycle such that the average inductor current follows the DAC reference signal.
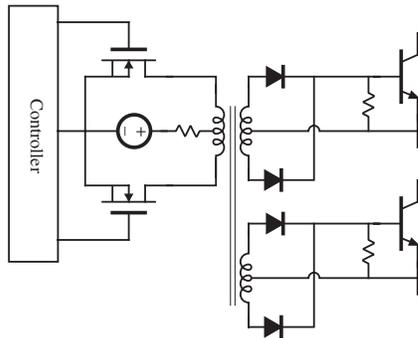

Figure 6. Unfolder base drive circuit using high-frequency dc transformer

Other digital control circuitry produces a sinusoidal reference that is synchronized to the ac line voltage. A digital maximum power point tracker (MPPT) and a multiplier adjust the amplitude of the sinusoidal reference such that the PV array operates at its maximum power point.

A supervisory controller implements the grid interface requirements of IEEE Standard 1547 [12]. The controller algorithms shut down the inverter when they detect that the ac line voltage or frequency lie outside of required tolerances. Additionally, they prevent unintentional islanding, and they shut down the inverter when abnormal fault conditions are detected.

An unfolder driver controls the slow inverter transistors to switch at the zero crossings of the ac line voltage waveform. This circuit behaves as a dc transformer to produce the required base drive current. Small high-frequency transformers provide floating drives to the unfolder transistors. Figure 6 illustrates one half of this circuit, driving diagonally-opposite transistors of the unfolder. The controller alternately drives small MOSFETs on and off at a high frequency, with dead times of a few hundred nanoseconds to prevent cross-conduction. The slow bipolar-junction transistors (BJTs) remain conducting during the dead times, and turn off after the controller ceases switching the MOSFETs.

IV. SIMULATION

A detailed MATLAB simulation was developed, to model losses, the ac line current spectrum, and control algorithms. This simulation was then used to compare alternative approaches as discussed in Section II. Key assumptions and supporting modeling details are documented in this section, and predicted waveforms are given.

The MATLAB sampled data model computes each switching subinterval using a single time step. The inductor current at the end of the subinterval is expressed as the initial current, plus a change given by the applied inductor voltage, multiplied by the subinterval length and divided by the inductance. The simulator detects discontinuous conduction mode, as well as duty cycle saturation, and adjusts accordingly. MOSFET, diode, inductor, and capacitor conduction loss energies are computed for each subinterval. These energies are summed over a complete ac line period and divided by the period to find the average power loss.

The conduction losses of Table I were computed for a 210 V dc input, a 25 W ac output, at 60 Hz and 120 V rms. The following conduction loss parameter values were used:

MOSFET on-resistance $R_{on} = 1.75\ \Omega$
Buck diode forward voltage drop $V_F = 1.1$ V
Buck CCM inductor dc resistance $R_L = 5.48\ \Omega$ total
Buck CCM inductance $L = 3.78$ mH
Switching frequency $f_s = 130$ kHz
Forward voltage drop of D_2 $V_{D2} = 1$ V
ESR of C_1 (energy storage capacitor) $R_{C1} = 0.71\ \Omega$
ESR of C_2 (filter capacitor) $R_{C2} = 4.25\ \Omega$
Total series resistance of EMI filter = 1.28 Ω
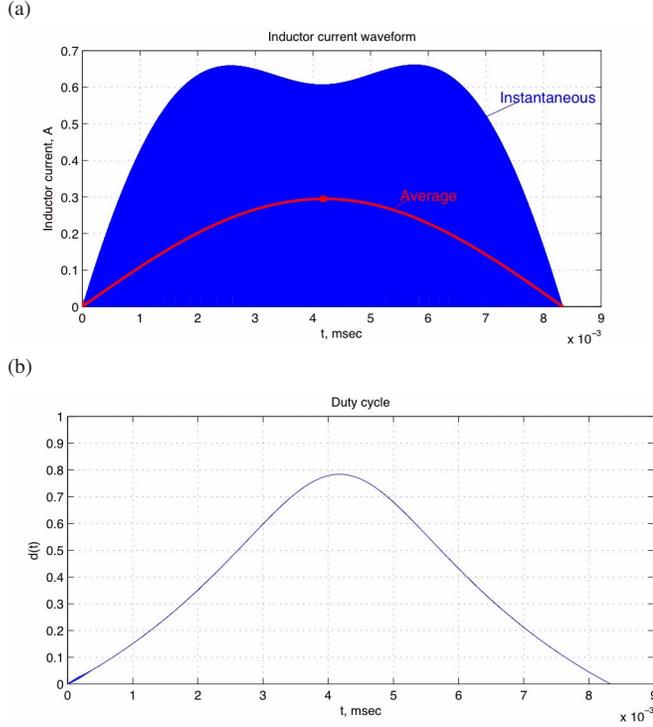
(a)

(b)

Figure 7. Simulated waveforms, DCM design operating at 25 W output power: (a) instantaneous and average inductor current, (b) duty cycle.

The DCM simulation of Table II employed the same element values, except the inductance was reduced to $L = 400~\mu$H, with a dc resistance of $R_L = 3.36~\Omega$. The above values were based on commercial datasheets of elements used in preliminary designs.

The approach used to model switching losses was based on [16]. Switching loss induced by diode reverse recovery was modeled by

$$E_{sw} = k_{tr}V_{pv}i_L^{1.25} + k_{Qr}V_{pv}i_L^{0.5} \tag{1}$$

where i_L is the inductor current during the MOSFET turn-on transition and V_{pv} is the PV panel voltage. The coefficients k_{Qr} and k_{tr} were estimated from the datasheet of the 400 V 1 A MURA140 ultrafast diode, and were taken as

$k_{Qr} = 105.6$ ncoul/A
$k_{tr} = 65$ ns/A$^{0.25}$

This constitutes the dominant loss in CCM, but is absent in DCM.

Switching losses induced by the MOSFET and diode nonlinear output capacitances were also modeled, using the approach described in [17]. The energies lost when the the MOSFET turns on are given by equations of the form

$$E_C = \frac{4}{3}\,C_0V_{pv}^{1.5} \tag{2}$$

where the constant C_0 is related to the small-signal output capacitance C specified by the datasheet at voltage V accord-

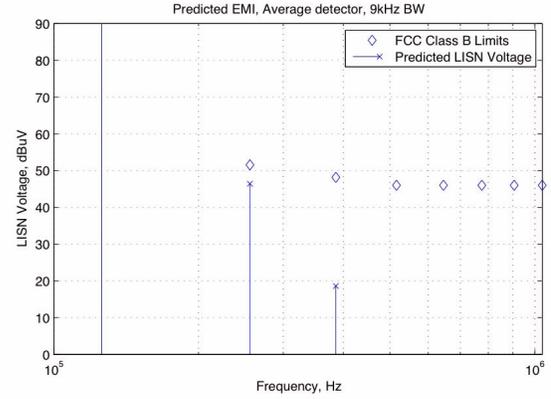
Figure 8. Predicted conducted EMI vs. FCC limits, for DCM design at 25 W with two-section EMI filter.

ing to:

$$C_0 = C\sqrt{V} \tag{3}$$

The 400 V 1.5 A MOSFET FQP3N40 has a specified output capacitance of 39 pF at 25 V, and the MURA140 has a specified capacitance of 5 pF at 25 V. This switching loss is smaller than the reverse recovery loss in CCM, but becomes the dominant switching loss in DCM.

Unfolder conduction loss and base driver power were based on experimentally measured values, and do not depend on the operating mode. A fixed allowance of 50 mW was budgeted for the controller power consumption. The power consumption of the MOSFET gate driver was taken to be four times the energy lost in the gate capacitances per switching period.

In continuous conduction mode, the simulation implements the digital average current control of [13,14]. In discontinuous conduction mode, the simulator employs a modification of the digital current control of [15].

Selected simulation waveforms are illustrated in Fig.7. Figure 7(a) shows the instantaneous DCM inductor current and its low-frequency average. Figure 7(b) contains the required duty cycle waveform, as generated by the controller.

The simulation additionally computes the ac line current harmonics, using a method similar to [19]. The Laplace transform of the inductor current and the LISN current are found at each simulation subinterval and evaluated numerically. The Laplace transform of a subinterval inductor current having linear ripple is given by:

$$i(s) = \left[\frac{i_0}{s} + \frac{i_1 - i_0}{s^2 t_1}\left(1 - e^{-st_1}\right) - \frac{i_1}{s}e^{-st_1}\right]e^{-st_0} \tag{4}$$

Here, i_0 is the current at the beginning of the subinterval at time t_0, and i_1 is the current at the end of the subinterval. The subinterval length is t_1. To compute the Laplace transform of a harmonic having angular frequency ω, (4) is evaluated at $s =$

$j\omega$, and the result summed for every subinterval over an ac line cycle. MATLAB is well suited to this calculation. Determination of rms magnitudes for a 9 kHz frequency span lead to the conducted EMI values regulated by FCC Part 15 subpart B. The result for the DCM design with a two-section EMI filter is given in Fig. 8. The lines represent the current harmonic value, while the diamonds are the FCC limits. There is a tradeoff between low-frequency harmonic generation, EMI filtering, and loss in capacitor ESR. Nonetheless, acceptable designs were found using two- or three-section EMI filters.

V. EXPERIMENTAL RESULTS

A power stage experimental prototype has been built and tested, to provide proof of feasibility. A photo of this prototype is contained in Fig. 1. The printed-circuit board dimensions are 3" x 5", and the components are no taller than 3 mm. With a 201 VDC input and a 30.8 W output, the measured efficiency of the dc-dc buck converter and EMI filter was 97.3% at a 130 kHz switching frequency. The MATLAB-based loss model of Section IV. predicted a worst-case efficiency of 96.3% at the same operating point.

Figure 9 presents inverter waveforms measured in the laboratory, with a resistive load. A measured inverter output voltage waveform is illustrated in Fig. 9(a). The spectrum of this waveform is illustrated in Fig. 9(b). The measured THD is
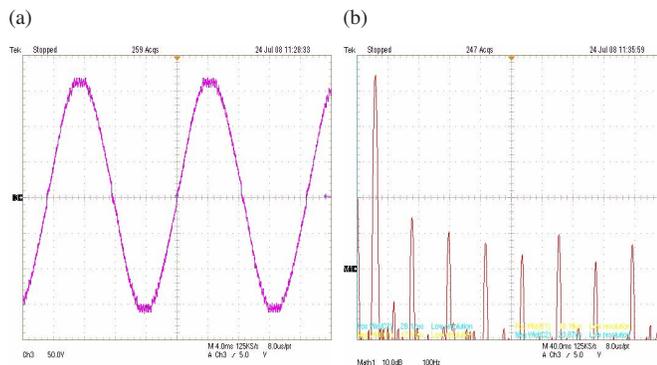

Figure 9. Measured bench-top inverter output: (a) voltage waveform, (b) spectrum.
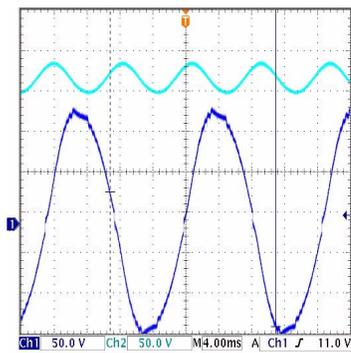

Figure 10. Measured waveforms with inverter powered by PV panel. Channel 1: ac output voltage. Channel 2: energy storage capacitor voltage.

Figure 11. Measured ac line current spectrum, grid tied and operating at rated power.

1.5%, with a third harmonic amplitude of 1.0%. The inverter was also connected to a PV panel and operated outside with a resistive load. Figure 10 contains measured waveforms under these conditions, including the inverter output voltage and the voltage of the energy storage capacitor.

Figure 11 illustrates the measured ac line current spectrum, with the inverter synchronized to the utility grid and producing an output power of 30 W. The measured total harmonic distortion was 4.9%, and the largest harmonic had an amplitude equal to 2.3% of the fundamental amplitude.

VI. CONCLUSIONS

The cost of power electronics is very low relative to the costs of PV cells and of installation today. Hence there is an opportunity to introduce power electronics to reduce the overall system costs of building-integrated PV systems. Meeting DOE goals of $3.25/W$_{pk}$ for PV systems in 2015 will require substantial integration of PV materials, power electronics, and interconnections into building materials that are easily and quickly installed, with a minimum of local engineering. This paper proposes a microinverter intended to satisfy these goals.

The requirements of very low profile, high temperature, and high efficiency operation require substantial changes to the traditional inverter technologies such as relatively low-frequency CCM operation and electrolytic energy storage capacitors. DCM operation is shown here to provide a viable solution, reducing both inductor value and switching loss by an order of magnitude. This approach cuts the predicted total loss in half and hence enables efficiencies exceeding 95% in an inverter having a profile of 3 mm. Additionally, the use of ceramic capacitors for 120 Hz energy storage is found to be feasible—with high-voltage X7R capacitors, the increased cost (9¢/W$_{pk}$ for 250 V or 630 V capacitors) is justified by the

125˚C rating and the potential reduction in installation costs. Increased volumes and offshore manufacturing may further reduce this cost.

The H-bridge topology is widely quoted in the literature of single-phase PV inverters. The CCM buck-plus-unfolder approach is also well known and has been previously proposed for (high profile back-of-the-panel) PV microinverters. While either approach can be employed here, the use of DCM requires a substantial differential-mode EMI filter, and this filter is significantly increased in size and cost when its components are ac rated. For this reason, we selected the buck-plus-unfolder approach, and placed the differential-mode EMI filter between the buck converter and the unfolder. This filter is realized using low-profile ceramic chip capacitors and small drum-core inductors.

The proposed approach can meet most standard PV grid interface requirements, including low line current THD and prevention of unintentional islanding. Nonetheless, it appears necessary to place a central box between the microinverter array and the utility. This box can include an ac disconnect switch, as well as transient protection and a smart grid or user computer interface. Placement of the major transient protection in a central box is beneficial from both cost and low-profile standpoints.

A substantial simulation system was developed using MATLAB. This simulation provided a detailed prediction of losses, and supplied the quantitative evidence to support the conclusions set forth here. These models of conduction loss and switching loss are based on datasheet parameters, and the predictions at dc operating points match experimental measurements well. A basic DCM buck converter power stage was found experimentally to exhibit an efficiency exceeding 97% at a nominal dc operating point; this stage is the core of the proposed approach. The tradeoff between conducted EMI, low-frequency line current harmonics, and filter capacitor loss is key to design of the buck-plus-unfolder approach; the simulation leads to informed design of the EMI filter to effectively resolve this tradeoff.

A laboratory prototype provides proof of the feasibility of this application and the proposed approach. The power stage, average current controller, and digital system controller have been demonstrated under grid-tied conditions. All power stage components exhibited a profile of 3 mm or less, and the system produced an ac line current having a THD of 4.9% at rated power.

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