Electrified Automotive Powertrain Architecture Using Composite DC-DC Converters

Hua Chen, Student Member, IEEE, Hyeokjin Kim, Student Member, IEEE,
Robert Erickson, Fellow, IEEE, and Dragan Maksimović, Fellow, IEEE

Abstract—In a hybrid or electric vehicle powertrain, a boost dc-dc converter enables reduction of the size of the electric machine and optimization of the battery system. Design of the powertrain boost converter is challenging because the converter must be rated at high peak power, while efficiency at medium to light load is critical for the vehicle system performance. By addressing only some of the loss mechanisms, previously proposed efficiency improvement approaches offer limited improvements in size, cost and efficiency trade-offs. This paper shows how all dominant loss mechanisms in automotive powertrain applications can be mitigated using a new boost composite converter approach. In the composite dc-dc architecture, the loss mechanisms associated with indirect power conversion are addressed explicitly, resulting in fundamental efficiency improvements over wide ranges of operating conditions. Several composite converter topologies are presented and compared to state-of-the-art boost converter technologies. It is found that the selected boost composite converter results in a decrease in the total loss by a factor of two to four for typical drive cycles. Furthermore, the total system capacitor power rating and energy rating are substantially reduced, which implies potentials for significant reductions in system size and cost.

Index Terms—DC-DC converter, composite converter, boost converter, electric vehicle power train

I. INTRODUCTION

A hybrid or electric vehicle power train includes a battery system, a motor drive system and, in some cases, a bidirectional dc-dc converter placed between the battery and the motor drive, as shown in Fig. 1. The boost dc-dc converter enables independent optimization of the battery system and a reduction in the size of the electric machine [1], [2]. The motor-drive dc bus voltage can be increased, which allows extensions of the motor speed range without field weakening. This improves both the motor and the inverter efficiency [3]. The converter can also dynamically adjust the dc bus voltage, so that the system efficiency can be further optimized [4]. The powertrain architecture using a dc-dc converter has been successfully incorporated in commercial vehicle systems [1], [5]–[7].

The losses associated with the boost dc-dc converter must be sufficiently low, so as to not compromise the advantages offered by the powertrain architecture shown in Fig. 1. Designing a high efficiency boost converter in this application is challenging, because the converter must be rated at high peak power, while efficiency at medium to light load is critical for the vehicle system performance. Various approaches have been proposed to improve the boost converter efficiency, including different methods to reduce switching losses [8]–[15], different methods to improve magnetics [16]–[21], and approaches to utilize devices with lower voltage rating [22], [23]. By addressing only some of the loss mechanisms, the previously proposed efficiency improvement approaches have offered limited improvements in size, cost and efficiency trade-offs. A new composite boost converter architecture has been introduced in [24]–[26]. This approach utilizes several smaller converter modules combined together to process the total system power; effectively, this approach is a modular multilevel system employing dissimilar module types. Each converter module processes a fraction of the system power, with effective utilization of the semiconductor and reactive elements. The ability to optimize each module independently at certain critical operating points leads to substantially increased average efficiency. Depending on operating conditions, the modules can operate in shut down or pass through modes to further reduce ac power losses. Overall, the loss mechanisms associated with indirect power conversion are addressed explicitly, resulting in fundamental efficiency improvements over wide ranges of operating conditions.

The objectives of this paper are to explain the challenges associated with the dc-dc converter design in automotive powertrain applications, to introduce several composite converter topologies, and to compare these approaches to existing state-of-the art solutions. The reasoning is based on the following postulates and assumptions:

• The power electronics system is loss-limited. Hence the ratio of output power to loss power is the key metric governing power density, cost of cooling system, and related performance.
• Average loss over typical driving cycles is substantially impacted by the low-power efficiency of the power electronics. Improvement of the light-load efficiency can substantially impact the net power loss.
• Total capacitor size significantly impacts the system size and cost, and is driven by the rms currents imposed on the capacitors by the power converters.
• The significant ongoing research in power electronics packaging and interconnects will enable the practical deployment of more complex circuit topologies.

The key conclusion is that it is possible to reduce the average loss by a factor of approximately four, while also reducing capacitor size by a factor of approximately two, through the
use of a composite converter approach. By contrast, existing soft-switching, multilevel, or coupled-inductor approaches either lead to only incremental improvements in efficiency, or require a substantial increase in capacitor size.

The paper is organized as follows: Section II describes the automotive powertrain application, explains the need to achieve high efficiency over wide ranges of conversion ratios and over wide ranges of power, and identifies dominant loss mechanisms in the conventional boost converter. Previous approaches to boost converter efficiency improvements are summarized in Section III. In Section IV, based on the concepts of direct and indirect power in dc-dc converters, several composite converter topologies are introduced to explicitly address the dominant loss mechanisms associated with indirect power conversion. A detailed comparison of the composite converters and the state-of-the-art approaches is presented in Section V based on loss models calibrated by experimental results. It is shown that one of the boost composite converters can result in reduction of the total loss over typical drive cycles, by a factor of two to four. Furthermore, the total system capacitor power and energy ratings are substantially reduced. Section VI concludes the paper.

II. ELECTRIFIED AUTOMOTIVE POWER TRAIN

Figure 1 shows the basic vehicle powertrain architecture with the bi-directional boost dc-dc converter. Variations of this architecture can be found in hybrid and electric vehicles. The dc-dc converter boosts the battery voltage, so that a higher-speed machine can be used, which has smaller size and higher efficiency. For example, in the 2010 Prius, the battery nominal voltage is approximately 200 V, and the DC-DC converter boosts the dc bus voltage to approximately 650 V [7].

In vehicular powertrain applications, the system is typically thermally limited. In other words, for a given thermal management design, the allowed average power loss is limited. For such systems, the ratio of output power to power loss

$$ Q = \frac{P_{out}}{P_{loss}} = \frac{\eta}{1 - \eta} $$

(1)

presents a more meaningful performance metric than efficiency $\eta$. By analogy with the quality factor of a reactive element, we define $Q$ of a power converter as the ratio of loss to output power. Fig. 2 shows the $Q = P_{out}/P_{loss}$ metric as a function of efficiency $\eta$. For example, if the system average efficiency is improved from 96% to 98%, the system average efficiency is improved by just 2%, which appears to be incremental. However, $P_{out}/P_{loss}$ is more than doubled. A technology that can achieve a doubling of $Q$ could enable doubling of the output power in a thermally limited system or could process the same output power while allowing the system cooling effort to be halved. These are substantial and non-incremental system-level improvements. High efficiency power electronics not only improves the system average efficiency such as miles per gallon equivalent (MPGe), but also increases the power density and significantly reduces the size and cost of the thermal management system.

In traditional power electronics applications, converter efficiency at full power is often critical. However, in electric powertrain applications, converter efficiency at intermediate and low power levels is actually more important. As an example, Fig. 3a shows the NREL ADVISOR [27] simulation result for a Ford Focus electric vehicle under different standard Dynamometer Drive Schedules (DDS) specified by the United States Environmental Protection Agency (EPA) [28]. The Urban Dynamometer Drive Schedule (UDDS) is a relatively
light load test that represents city driving conditions. The Highway Fuel Economy Test (HWFET) is a highway driving cycle with maximum 60 mph speed. US06 is a supplemental test procedure, which includes fast acceleration events in an aggressive driving cycle. Figure 3b shows the corresponding distribution of the normalized vehicle power. As shown in Fig. 3b, even in the most aggressive US06 driving profile, most of the time the vehicle operates at less than 40% of its maximum power.

![Vehicle speed and normalized power vs. time](image1)

![Vehicle normalized power histogram](image2)

Fig. 3. Simulation of a typical Ford Focus electric vehicle with NREL ADVISOR simulator

In this work, a 30 kW boost dc-dc converter is considered. The battery voltage $V_{battery}$ varies from 150 V to 300 V, with a nominal voltage of 200 V. The boost conversion ratio $M = V_{bus}/V_{battery}$ can vary from 1 to 4. With inclusion of all transients, the worst-case dc bus voltage $V_{bus}$ is limited to 800 V. With a 33% voltage derating, 1200 V semiconductor devices are required in the conventional boost dc-dc converter. Under the worst-case conditions (30 kW at 150 V battery voltage, with conversion ratio of $M = 1$), the boost switches conduct 200 A current. 1200 V silicon IGBTs are typically employed. As a representative example, the Fuji Electric 2MBI200VB-120-50 2-pack IGBT module is considered. This is a 1200 V 200 A punch-through IGBT with co-packaged diode. Curve-fitted device loss models are summarized in Table I. The transistor conduction loss is modeled as

$$P_Q = I_{on}V_{ces} + I_{on}^2R_I$$  \hspace{1cm} (2)

where $I_{on}$ is the device conducting current. Similarly, the diode conduction loss is modeled as

$$P_D = I_{on}V_f + I_{on}^2R_D$$  \hspace{1cm} (3)

The IGBT turn-on switching loss is modeled as

$$P_{on} = K_{on}f_{sw}V_{hes}V_{off}f_{sw}$$  \hspace{1cm} (4)

where $f_{sw}$ is the switching frequency, and $V_{off}$ is the IGBT off-state blocking voltage. Similarly, the IGBT turn-off loss is modeled as

$$P_{off} = K_{off}f_{on}V_{hes}V_{off}f_{sw}$$  \hspace{1cm} (5)

and the diode reverse-recovery loss is modeled as

$$P_{rr} = K_{rr}f_{on}V_{hes}V_{off}f_{sw}$$  \hspace{1cm} (6)

Table I

<table>
<thead>
<tr>
<th>Part number</th>
<th>Rating</th>
<th>Switching frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>2MBI200VB-120-50</td>
<td>1200 V / 200 A IGBT</td>
<td>10 kHz</td>
</tr>
</tbody>
</table>

Table II

<table>
<thead>
<tr>
<th>Semiconductor</th>
<th>Part number</th>
<th>Rating</th>
<th>Switching frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductor</td>
<td>2MBI200VB-120-50</td>
<td>1200 V / 200 A IGBT</td>
<td>10 kHz</td>
</tr>
</tbody>
</table>

**Fig. 4a** shows the efficiency of a typical conventional boost converter at $V_{battery} = 200$ V and $V_{bus} = 650$ V, as a function of output power level. The conventional boost converter efficiency is 96% to 96.4% at medium load to full load, but efficiency drops drastically at light load. **Fig. 4b** shows the normalized loss breakdown of this boost converter. Ac losses, including semiconductor switching losses $P_{sw}$ and inductor ac losses $P_{indAC}$, dominate the total loss at light to
medium loads. Therefore, to improve the converter efficiency at medium to light load range, which is very important given the power distribution for typical driving cycles, it is necessary to reduce the converter ac power losses.

III. REVIEW OF APPROACHES TO BOOST CONVERTER EFFICIENCY IMPROVEMENTS

This section summarizes several approaches proposed to improve efficiency of the boost dc-dc converter in electrified vehicle powertrain applications. In Section V these approaches are compared with the boost composite converters introduced in Section IV.

A. Soft switching approaches

Various soft switching techniques, such as zero-voltage switching (ZVS) or zero-current switching (ZCS) have been investigated extensively in power electronics applications. Since the switching loss contributes significantly to the total loss in the conventional boost converter, it is of interest to investigate effectiveness of soft switching approaches. In practice, a soft switching technique may reduce but not completely eliminate switching loss. This is especially the case considering minority carrier devices such as IGBTs, where losses associated with turn-off current tailing can be reduced but not eliminated. Furthermore, auxiliary circuits introduced to facilitate soft switching introduce new additional losses. To evaluate the effectiveness of switching loss reduction, a soft-switching efficiency \( \eta_{ss} \) can be defined as:

\[
\eta_{ss} = 1 - \frac{P_{sw,ss}}{P_{sw}}
\]

where \( P_{sw} \) is the switching loss in the original hard-switched converter, and \( P_{sw,ss} \) is the remaining switching loss after adopting soft switching. Ideally \( \eta_{ss} = 100\% \), meaning that all of the switching loss is recovered. In practice, \( \eta_{ss} \) is always less than 100%.

The snubber-assisted zero-voltage transition / zero-current transition (SAZZ) approach [8]–[11] is an extension of the well-known auxiliary resonant commutated pole concept [29]. The SAZZ approach addresses some of the switching loss mechanisms, including turn-on losses due to diode reverse recovery and, to some extent, turn-off losses due to IGBT current tailing. The auxiliary circuit is relatively simple, and the converter main switch stresses and conduction losses remain the same as in the original boost converter.

Reference [8] describes a 200 V to 400 V 8 kW SAZZ boost prototype achieving 96% efficiency when operating at 100 kHz using MOSFETs. Its power stage schematic is shown in Fig. 5. A 250 V to 390 V 25 kW bi-directional non-inverting SAZZ buck-boost prototype using 600 V IGBTs is presented in [9], achieving 97.4% efficiency at full output power. The SAZZ concept is extended in [10] using a modified snubber configuration and saturable inductors in the snubber circuit. The prototype demonstrates efficiencies exceeding 98.5% at 8 kW to 15 kW output power with 300 V to 420 V conversion, using 600 V MOSFETs operating at 50 kHz. Reference [11] reports another variation of the SAZZ concept, based on three interleaved unidirectional modules connected in parallel. A 200 V to 400 V conversion is demonstrated at up to 15 kW per module, with 30 kHz switching frequency using 1200 V IGBT.
[11], it can be estimated that the SAZZ approach with IGBT devices yields $\eta_{SAZZ} \approx 38\%$.

B. Coupled inductor approaches

Approaches based on parallel interleaved topologies and coupled inductors can be used to reduce magnetic losses and, to some extent, switching losses [16]–[21]. Paralleled boost converters with coupled inductors have been studied in a number of references, including [16]. Interleaving reduces the rms current applied to the output capacitor, and allows operation at reduced switching frequency, which results in reduced switching losses. Furthermore, reference [16] also points out that soft-switching can be achieved with the help of the leakage inductance associated with the coupled inductors.

A particularly interesting coupled-inductor approach is introduced in [17] and illustrated in Fig. 6, which shows the schematic of a bi-directional version of the proposed coupled-inductor boost converter. With this approach, each phase only carries half of the total current, and the switching frequency is equal to one half of the inductor current ripple frequency. Therefore the device switching loss is reduced. Furthermore, thanks to the 1:1 transformer, the volt-seconds applied to the inductor are reduced so that the inductor loss can be reduced. However, there are additional losses associated with the transformer. In similar approaches and extensions [18]–[20] all magnetic components are integrated on the same core, which may lead to a higher power density and a reduction in total magnetic losses.

The unidirectional prototype demonstrated in [17] has an input voltage range of 70 V to 180 V, and an output voltage range of 210 V to 252 V, with a maximum power of 42 kW. The switches are realized using the APTC60DAM18CTG power module composed of one 600 V MOSFET and one 600 V SiC Schottky diode. The switching frequency is 45 kHz. With a fixed boost ratio of 1.4, the experimentally measured peak efficiency is 98.4% at approximately 17 kW output power. Over 98% efficiency is achieved from 8 kW to 32 kW output power.

C. Three-level converter approach

Three-level converters [22], such as the bi-directional three-level boost converter using MOSFETs shown in Fig. 7, have been introduced to allow use of switches with voltage rating reduced by a factor of two. Furthermore, similar to the coupled-inductor approach in [17], inductor volt-seconds are reduced and the switching frequency is equal to one half of the inductor current ripple frequency. As a result, the inductor size and inductor losses can be reduced.

The bidirectional three-level boost converter of Fig. 7 can be considered a candidate for the automotive powertrain application. Since the device voltage stress is equal one half of the bus voltage, 600 V MOSFETs can be used to allow higher switching frequency, and substantial reductions in the inductor size and losses. With MOSFETs, however, the requirement of bi-directional power flow constrains the design to utilize MOSFETs body diodes, instead of fast external diodes, which raises concerns about switching losses associated with diode reverse recovery. Furthermore, the flying capacitor is exposed to large rms current. These issues are further addressed in the comparison of approaches in Section V.

D. Z-source inverter approach

The Z-source (or impedance-source) inverter [30] and its many variations such as [31], [32], present an interesting alternative to conventional cascaded converter and inverter approaches shown in Fig. 1. Figure 8 shows a typical three-phase Z-source inverter with bi-directional power capability. It integrates the functionality of a boost dc-dc converter stage and an inverter stage. While the conventional buck-type voltage-fed inverter is only capable of producing output voltages lower than the bus voltage, the Z-source inverter is capable of producing output voltages either higher or lower than the input voltage. Therefore this approach may be suitable for the considered powertrain application. For example, [33], [34] demonstrated Z-source inverters intended for a fuel cell hybrid electric vehicle (FCHEV) powertrain.

A very interesting feature of the Z-source inverter is that it is immune to shoot-through failures. The shoot-through state when both a high-side and a low-side switch turn on at the same time is in fact utilized to achieve the boost function. The buck inverter and the boost functions are effectively
Fig. 8. Bi-directional three-phase Z-source inverter

time-multiplexed into three-phase PWM signals. However, this time-multiplexing operation is also the root cause of some limitations of the Z-source inverter. For example, in the conventional approach where the boost converter is cascaded with a three-phase inverter, as shown in Fig. 1, the boost stage output bus voltage is $V_{bus} \geq V_{battery}$. With modulation schemes such as space vector pulse-width modulation (SVPWM), at the moment when one leg of the inverter operates with duty cycle $D = 1$, and another leg operates with duty cycle $D = 0$, the line voltage amplitude $V_{La} = V_{bus}$ can be achieved. In the Z-source inverter, however, to achieve the same $V_{La} > V_{battery}$, the shoot-through state has to be used to achieve the voltage boost. Because the shoot-through state extends over a time interval during each switching period for all three inverter legs, none of the legs can be operated at $D = 1$, which means that the average output voltage of each leg has to be obtained from a voltage higher than $V_{La}$. To achieve the same line voltage amplitude $V_{La} > V_{battery}$ as in the conventional approach, it can be shown that the device voltage rating has to be at least $V_{B} = 2V_{La} - V_{battery}$. Considering the powertrain example where the boost dc-dc converter is able to produce 800 V output voltage at 200 V input voltage, 800 V line voltage amplitude can be produced in the conventional architecture of Fig. 1. Devices rated at 1200 V can be applied. To produce the same line voltage amplitude at 200 V input with the Z-source inverter, the device voltage stress is 1400 V. Using the same device voltage derating, the Z-source inverter would require 2100 V devices.

The time-multiplexing operation also implies that the devices in the Z-source inverter must conduct higher currents resulting in potentially higher conduction losses, even though the Z-source inverter has fewer devices compared to the conventional approach.

Similar considerations and conclusions have been reached in [35] in a wind turbine application. Reference [34] shows that at operating points having very small voltage boost ratios, the Z-source inverter can theoretically offer slight efficiency improvements. In [36], where the Z-source inverter efficiency is evaluated in an electric vehicle powertrain application over a practical driving profile, it was found that the conventional approach results in a slightly higher efficiency.

IV. Composite converter architecture

As discussed in the previous section, various existing approaches to converter efficiency improvements partially address some of the loss mechanisms. As such, they tend to result in incremental or partial improvements in size, cost and efficiency trade-offs. The objectives of this section are to first identify the fundamentals of loss mechanisms and then to introduce composite converter configurations where the loss mechanisms are directly addressed, and which can lead to substantial, non-incremental improvements in efficiency and $P_{out}/P_{loss}$ figures of merit.

Fig. 9. Conventional boost converter: (a) power stage schematic; (b) averaged switch model

Consider again the conventional boost converter shown in Fig. 9a, with transistor $Q_1$ voltage and current waveforms
shown in Fig. 10a.

The instantaneous switch voltage \( v_{Q1}(t) \) can be decomposed into the average dc component \( \langle v_{Q1} \rangle \), and the ac component \( \tilde{v}_{Q1}(t) \), as shown in Fig. 10b. The same can be applied to all switch voltages and currents, as follows:

\[
\begin{align*}
  v_{Q1}(t) &= \langle v_{Q1} \rangle + \tilde{v}_{Q1}(t) \\
  i_{Q1}(t) &= \langle i_{Q1} \rangle + \tilde{i}_{Q1}(t) \\
  v_{Q2}(t) &= \langle v_{Q2} \rangle + \tilde{v}_{Q2}(t) \\
  i_{Q2}(t) &= \langle i_{Q2} \rangle + \tilde{i}_{Q2}(t)
\end{align*}
\] (8)

With the assumption that the switches are lossless, the switch power can be expressed as:

\[
p_{Q1}(t) = v_{Q1}(t) i_{Q1}(t) = 0
\] (9)

By substituting (8) into (9), and taking the average over one switching period, we obtain

\[
\frac{1}{T_s} \int_0^{T_s} \langle (v_{Q1}) + \tilde{v}_{Q1}(t) \rangle \langle (i_{Q1}) + \tilde{i}_{Q1}(t) \rangle \, dt = 0
\] (10)

Since the average of each ac component over one switching period is zero, (10) can be re-arranged as:

\[
\langle v_{Q1} \rangle \langle i_{Q1} \rangle = DV_{in}I_{in} = -\frac{1}{T_s} \int_0^{T_s} \tilde{v}_{Q1}(t) \tilde{i}_{Q1}(t) \, dt
\] (11)

Similarly, for \( Q_2 \):

\[
-\langle v_{Q2} \rangle \langle i_{Q2} \rangle = \langle \tilde{v}_{Q2}(t) \tilde{i}_{Q2}(t) \rangle
\] (12)

Equations (11) and (12) can be interpreted as follows: switch power \( \langle \tilde{v}_{Q1}(t) \tilde{i}_{Q1}(t) \rangle \), i.e., \( Q_1 \) operates as an inverter. Similarly, \( Q_2 \), which operates as a rectifier, converts the ac average power back into dc power. The effective dc-to-ac-to-dc power conversion associated with the switches \( Q_1 \) and \( Q_2 \) leads to the notion of ac or indirect power, which is fundamental to all dc-dc converters [37]. In the boost converter, the ac power is \( P_{\text{indirect}} = DV_{in}I_{in} \). The averaged switch model shown in Fig. 9b [38] can be used to examine the voltage step-up and power flow in the converter. The voltage conversion ratio is

\[
M = \frac{V_{out}}{V_{in}} = 1 + \frac{D}{D'} = 1 - \frac{1}{M'}.
\] (13)

The output power can be written as a sum of the ac or indirect power \( P_{\text{indirect}} = V_{in}(D'I_{in}) = DP_{out} \) delivered through the ideal dc transformer in the averaged switch model, and the direct power \( P_{\text{direct}} = V_{in}(D'I_{in}) = DP_{out} \) delivered directly from input \( V_{in} \) to output \( V_{out} \),

\[
P_{out} = P_{\text{direct}} + P_{\text{indirect}} = DP_{out} + DP_{out}.
\] (14)

Combination of (13) and (14) implies that

\[
P_{\text{indirect}} = P_{out} \left(1 - \frac{1}{M}\right)
\] (15)

Note that \( P_{\text{indirect}} \) represents the portion of power actively processed by the converter switches, and is therefore subject to both switch and inductor conduction (dc losses) and semiconductor switching losses and inductor ac losses (ac losses). Conversely, \( P_{\text{direct}} \) is transferred directly and is subject only to dc conduction losses, which can be relatively low. Importantly, it follows that the converter efficiency is fundamentally limited by the amount of indirect power processed, and by the efficiency of indirect power processing. In particular, as shown in Section II, this is the case in electrified automotive powertrain applications where ac losses dominate and light-to-medium load efficiency is very important.

As implied by (15) for the boost converter, \( P_{\text{indirect}} \) is determined by the conversion ratio \( M \). Therefore, as is well understood and confirmed in practice, it is difficult to construct a high-efficiency converter with a large step-up ratio \( M \). An example is given in Fig. 11. The direct / indirect power is calculated for a conventional boost converter at fixed 5 kW output power, with different conversion ratios, in Fig. 11a. The dc and ac power loss is modeled in Fig. 11b. The ac power loss is strongly correlated to indirect power, while the dc power loss increases as indirect power increases as well. While discussed here in the context of the boost converter, these considerations apply to dc-dc converters in general [37].

One may note that various soft-switching techniques and other approaches reviewed in Section III can be interpreted as attempts to improve efficiency of indirect power processing. A fundamentally different approach is based on composite converter architectures consisting of dissimilar partial power processing modules where high conversion ratios can be obtained by stacking modules in series or parallel, and where indirect power processing is delegated to dedicated highly-efficient modules, while regulation is accomplished using modules processing low or no indirect power [24]–[26].
One approach to improve efficiency of indirect power processing is to utilize an unregulated “DC transformer” (DCX) module, such as the converter shown in Fig. 12. If the secondary-side switches are passive diodes or synchronous rectifiers emulating diode operation, this circuit is a simple DCX, which provides an essentially fixed voltage conversion ratio $N_{DCX}$ at very high efficiency [39]. If the secondary side switches ($M_{S1}–M_{S4}$) are actively controlled, the circuit is referred to as the Dual-Active Bridge (DAB) [40]. Importantly, the converter can be optimized to achieve soft switching and low conduction losses at operating points where the transformer currents are trapezoidal [41]–[43].

Since the DCX can process the indirect power more efficiently, the indirect power path in the boost converter modeled as shown in Fig. 9b can be replaced by the DCX. Replacing the ideal dc transformer with the DCX circuit results in the configuration shown in Fig. 13. This converter can be regarded as a DCX connected as an auto-transformer. The modeled efficiency of an example design is shown in Fig. 14. Although the DCX is designed with 1200 V IGBTs, a remarkable improvement in efficiency can be observed, compared to the conventional boost converter. The efficiency improvement at medium to light load is more significant, which is because DCX processes indirect power in an efficient way so that the ac power loss is reduced.

The circuit shown in Fig. 13 is not a practical converter, because it only works at one fixed voltage conversion ratio, and the dc bus voltage cannot be regulated. In the following subsections, several practical composite converter topologies are developed. The composite converters combine a DCX module with other common converter modules such as buck, boost, or non-inverting buck-boost converter. Each converter module is only required to process partial power, and can be operated at higher efficiency. The modules are also designed in a way so that most of the indirect power is processed by the DCX. Therefore the rest of the modules operate with conversion ratio close to one, at a much higher efficiency. Furthermore, each module can also be optimized independently to enhance efficiency at certain critical operation conditions. The use of lower voltage rating devices allows additional performance improvements, in terms of reduced on-resistance and switching loss. Finally, it is shown that the composite converter approach has potentials to reduce significantly the system capacitor rating, which can result in reduced system volume and reduced cost.

### A. Boost Composite Converter A

Fig. 15 shows a boost composite converter based on Fig. 13, but with a non-inverting buck-boost converter module inserted to control the DCX voltage. If we denote the non-inverting buck-boost converter voltage conversion ratio as $M_{bb}(D)$, and DCX turns ratio as $N_{DCX}$, then the two converters in series have the total voltage conversion ratio of $M_{bb}(D)N_{DCX}$, which emulates the duty cycle controlled ideal dc transformer in Fig. 9b. The overall voltage conversion ratio of this composite converter is:

$$M = \frac{V_{bus}}{V_{battery}} = 1 + M_{bb}(D)N_{DCX} \quad (16)$$

The non-inverting buck-boost module is operated as a buck module for $M_{bb} < 1$, and as a boost module for $M_{bb} > 1$. This results in much higher efficiency than operating the module as a buck-boost with all four devices switching [44]–[46]. The two operation modes: DCX + buck mode and DCX + boost mode, are shown in Fig. 16.

The composite converter inherits the merits from the configuration in Fig. 13. The direct power path is a direct loss-free short-circuit connection. However, similar to the configuration in Fig. 13, although this configuration does reduce the device voltage stress, the reduction is not sufficient to facilitate devices with much lower voltage rating. For example, when the battery voltage is 200 V, if 800 V is desired at the dc bus output, the DCX must produce 600 V output. In this case, 900 V or 1200 V devices would be required. If the DCX turns ratio $N_{DCX}$ is large enough, 600 V devices can be used in the non-inverting buck-boost module. Another drawback of this configuration relates to operation at low system conversion ratios: the non-inverting buck-boost converter must operate with a large step-down ratio. The inductor current equals the output current multiplied by $N_{DCX}$. As a result, reduced efficiency can be expected at reduced voltage conversion ratio.

### B. Boost composite converter B

To allow 600 V devices in all modules, the boost composite converter B is presented in Fig. 17. Instead of inserting the
non-inverting buck-boost converter before the DCX, the same converter is inserted on the input side of the system. The system overall voltage conversion ratio is

\[
M = \frac{V_{bus}}{V_{battery}} = M_{bb}(D)(1 + N_{DCX}) \quad (17)
\]

Notice that the composite converter B shares the same operating modes as converter A, as shown in Fig. 16. If the DCX conversion ratio is chosen to be \(N_{DCX} = 1\), the dc bus voltage stress can be shared evenly between the DCX primary side and the secondary side. Therefore the worst-case device voltage stress is equal to one half of the bus voltage and so 600 V devices can be used in all modules in the application that requires up to 800 V output bus voltage. A drawback of this configuration is that the non-inverting buck-boost module is required to process the full system power.
C. Composite converter topology C

Figure 18 shows another composite converter topology. Instead of controlling the DCX output voltage, a boost converter is added in the lower path to regulate the dc bus voltage. If we denote the boost voltage conversion ratio as $M_{\text{boost}}(D)$, the system voltage conversion ratio is

$$M = \frac{V_{\text{bus}}}{V_{\text{battery}}} = M_{\text{boost}}(D) + N_{\text{DCX}}$$  \hspace{1cm} (18)

Notice that for boost converter, $M_{\text{boost}}(D) \geq 1$. Therefore, to achieve a system conversion ratio $M < 1 + N_{\text{DCX}}$, it is required to shut down the DCX (with secondary-side switches shorting the DCX output port) and operate the boost converter alone. This leads to two different operation modes for composite converter C: DCX + boost mode and boost only mode, as depicted in Fig. 19.

In comparison with composite converter topology A, the boost module in topology C processes direct power as well as a part of the indirect power. But, in comparison with the conventional boost converter, the boost module processes much less indirect power, with much reduced conversion ratio, and therefore higher efficiency. On the other hand, at low conversion ratios, the boost only mode is more efficient than DCX + buck mode of the composite topologies A and B.

A drawback of composite converter C is that to transition from DCX + boost mode to boost only mode, the DCX module must be shut down abruptly and the boost output voltage must be increased accordingly. This may lead to some difficulties in control. Furthermore, since the DCX output voltage is not controlled, the device voltage stress reduction is relatively small. For the application considered here, the boost module and the DCX module must employ 1200 V devices.

The composite converter C architecture may be attractive in some low-voltage low-power applications where only a narrow input/output voltage range is required. Related configurations, resembling operation with reverse power flow in the modular C architecture, have been reported in [47], [48], where the DCX is implemented using multi-phase LLC resonant converters, and the boost converter is replaced with an isolated PWM converter. The device voltage sharing and the mode transition are less of a concern in the computing or telecommunication applications considered in [47], [48] target, with a relatively narrow voltage conversion range, and at lower operating voltages.

D. Composite converter topology D

To address the mode transition problem of composite converter C, the composite converter D is proposed, as shown in Fig. 20. A buck converter module is inserted before DCX module to control the DCX output voltage. The buck module output voltage can smoothly ramp down to zero so that the DCX module can be shut down gracefully. If we denote the buck module voltage conversion ratio as $M_{\text{buck}}(D_{\text{buck}})$, the total system conversion ratio is:

$$M = \frac{V_{\text{bus}}}{V_{\text{battery}}} = M_{\text{boost}}(D_{\text{boost}}) + M_{\text{buck}}(D_{\text{buck}})N_{\text{DCX}}$$  \hspace{1cm} (19)

It is not necessary to operate all converter modules together. When the system voltage conversion ratio $M$ is greater than $1 + N_{\text{DCX}}$, then the buck module can be operated in pass-through with $D_{\text{buck}} = 1$, and the system operates in DCX + boost mode. When $M < 1 + N_{\text{DCX}}$, the boost module can be operated in pass-through with $D_{\text{boost}} = 0$, and the system operates in DCX + buck mode. With the extra buck module, the DCX output voltage can be well controlled, and the dc bus voltage stress can be shared evenly between the DCX and boost modules. Hence 600 V devices can be employed.
in all converter modules, with 33% voltage derating. If we define the allowed maximum device voltage stress as \( V_{Q,\text{max}} \), when the battery voltage \( V_{\text{battery}} > V_{Q,\text{max}}/N_{\text{DCX}} \), and bus voltage \( V_{\text{bus}} > V_{\text{battery}} + V_{Q,\text{max}} \), the buck module can limit the DCX output voltage stress to \( V_{Q,\text{max}} \) and the system operates in DCX + buck + boost mode. On the other hand, when \( V_{\text{bus}} \leq V_{Q,\text{max}} \), the system can operate in boost only mode to improve efficiency at low voltage conversion ratios. The operating modes of the composite converter D are depicted in Fig. 21.

![Composite converter D operating modes](image)

Fig. 21. Composite converter D operating modes

It should be noted that the series combination of the buck and DCX modules of Fig. 20 could be replaced by a dual active bridge module. This would lead to a reduced switch count. However, we have observed higher laboratory efficiencies with the configuration shown in Fig. 20.

V. COMPARISON OF CONVERTER APPROACHES

In this section, the performance of different composite converter architectures are evaluated and are compared with prior boost converter approaches.

A. Generic comparison

For a given converter topology, the choices of semiconductor devices, switching frequency, magnetics design, and many other design parameters can result in very different physical designs. Nevertheless, it is beneficial to compare the different converter approaches in a more generalized way, in order to gain higher-level insights that guide design decisions.

To quantify the semiconductor device usage in different converter approaches, a specified device power rating is introduced as

\[
P_{Dn} = \frac{\sum I_{\text{device},\text{rms}} V_{\text{device, max}}}{P_{\text{out, max}}} \tag{20}
\]

which is the sum of all device rms currents multiplied by device voltage ratings, normalized to the converter maximum output power. This can be regarded as a measure of how well the power devices are utilized in a given converter topology.

Table III shows a comparison of the normalized total specified device power for the converter approaches considered in the previous sections, at a fixed voltage conversion ratio \( M = 3.25 \). At this voltage conversion ratio, with 200 V battery voltage, the bus voltage is 650 V, which is a typical operating point for the powertrain system. The calculation ignores the inductor current ripple, and therefore it is independent of the choice of magnetics, switching frequency, and device technology. Typical DCX transformer turns ratios \( N_{\text{DCX}} \) are chosen for the composite converter designs; these are optimized for the powertrain application. The data of Table III indicates that the soft-switching approach and the coupled inductor approach exhibit the same device power rating as the conventional boost converter, which implies that their designs may require the same total device semiconductor area. The three-level converter device power rating is slightly smaller than in the conventional boost converter. Although the composite approach requires increased power device component count, composite converter C and composite converter D show even smaller total device power ratings than the other approaches. This implies that the total semiconductor areas for the composite converters C and D could be similar to the other approaches, if not smaller. Table III also implies that the composite converters A and B may not utilize the semiconductor devices as efficiently as the other approaches.

![Normalized total device power comparison between Z-source inverter and conventional boost cascaded with inverter approach](image)

Fig. 22. Normalized total device power comparison between Z-source inverter and conventional boost cascaded with inverter approach

The Z-source inverter combines the functions of the boost DC-DC converter and the inverter. Therefore a separate comparison must be made to quantify the performance of the Z-source inverter. Figure 22 compares the total device power rating of Z-source inverter against the conventional boost converter cascaded by a standard inverter. For both cases, it is assumed that sinusoidal pulse-width modulation (SPWM) is employed in the inverter, and the load is assumed to have unity power factor. The normalized total device power rating is plotted against the battery-to-machine voltage conversion ratio \( V_{\text{Line},p/p} / V_{\text{battery}} \). Figure 22 implies that the semiconductor device utilization for Z-source inverter is relatively poor. For a given semiconductor device area, the Z-source inverter results in much larger device conduction losses, which agrees with conclusions in [35], [36].

To quantify the capacitor size for a given converter topology,
the normalized total capacitor power rating is defined as

\[
P_{\text{CN}} = \frac{\sum I_{\text{cap, rms - max}} V_{\text{cap, max}}}{P_{\text{out, max}}} \tag{21}\]

which is the sum of all capacitor rms current ratings multiplied by the capacitor voltage ratings, and is normalized to the converter maximum output power. In the electrified vehicle application, film capacitors are usually used, and the converter system is typically thermally limited. Therefore the capacitor size is usually limited by its rms current rating rather than its capacitance. Additionally, the voltage rating affects the size and cost of the capacitors as well. Therefore the total capacitor power rating reflects the size and cost of the capacitors in a given converter topology.

For example, in a conventional boost converter, let us assume that the inductor is very large, and the inductor current ripple is ignored. The output capacitor rms current is

\[
I_{\text{out, rms}} = I_{\text{in}} \sqrt{D(1 - D)}
\]

\[
\leq \begin{cases} 
\frac{P_{\text{out, max}}}{2V_{\text{in}}} & \text{for } M_{\text{max}} \geq 2 \\
\frac{P_{\text{out, max}}}{M_{\text{max}} - 1} \frac{V_{\text{in}}}{M_{\text{in}}} & \text{for } 1 \leq M_{\text{max}} < 2
\end{cases} \tag{22}
\]

The output capacitor voltage is

\[
V_{\text{out}} = V_{\text{in}} M_{\text{max}} \tag{23}
\]

Therefore the normalized total capacitor power rating of the conventional boost converter is

\[
P_{\text{CN}} = \frac{I_{\text{out, rms - max}} V_{\text{out, max}}}{P_{\text{out, max}}} = \begin{cases} 
\frac{M_{\text{max}}}{2} & \text{for } M_{\text{max}} \geq 2 \\
\frac{M_{\text{max}}}{M_{\text{max}} - 1} \frac{V_{\text{in}}}{M_{\text{in}}} & \text{for } 1 \leq M_{\text{max}} < 2
\end{cases} \tag{24}
\]

With the maximum voltage conversion ratio of \(M_{\text{max}} = 4\), specified, the conventional boost converter exhibits \(P_{\text{CN}} = 2\). Since the inductor current ripple is ignored in this analysis, the result is independent of inductor design, switching frequency, or device technology; it is simply the property of the converter topology itself. The normalized total capacitor power ratings of different converter approaches with maximum voltage conversion ratio \(M_{\text{max}} = 4\) are compared in Table IV. The capacitor power rating is reduced by a factor of two in the coupled-inductor approach, because it is basically an interleaved two-phase boost converter. Although the composite approach requires an increased capacitor component count, the composite converters A, B, and D can achieve a factor of two reduction in capacitor power rating reduction. Because composite converter C has a wider operation range of boost only mode, it requires a slightly larger capacitor power rating, although the rating is still 25% smaller than that of the conventional boost converter. It is important to note that the capacitor power rating of the three-level converter is two times larger than for the conventional boost approach, because of the high current stress in the additional flying capacitor. This is a significant disadvantage of the three-level boost converter in the electrified vehicle application.

These generic comparisons illustrate some fundamental properties of the considered converter approaches, which are independent of switching frequency and device technology. However, other factors such as device switching loss, and magnetics loss and size should also be considered in a practical design as well. Therefore, it is useful to compare different converter approaches using example physical designs, as described in the following sections.

**B. Composite converter comparisons**

To evaluate the performance of different composite converter topologies, each topology is designed with physical device models, and the efficiencies are compared. 30 kW dc-dc converter designs are considered, assuming a nominal 200 V battery voltage with a 150 V to 300 V worst case range. The voltage conversion ratio varies from 1 to 4, and the worst-case dc bus voltage is limited to 800 V.

In composite topology A, the worst-case voltage stress of the DCX secondary side is 600 V. For this design, a 1200 V 100 A IGBT module is assumed. The loss model of the 2MBII100VA-120-50 module from Fuji Electric is extracted from its datasheet and documented in Table V, with loss model equations following (2) – (6). With the DCX transformer turns ratio chosen to be \(N_{\text{DCX}} = 1.5\), the DCX primary side as well as the buck-boost converter voltage stress are 400 V, and therefore 600 V devices can be used. Silicon MOSFETs (Fairchild FCH76N60NF MOSFET die) are chosen. These are 600 V 46 A super-junction MOSFETs with fast recovery body diodes. The extracted loss model is documented in Table VI. The MOSFET conduction loss is modeled as

\[
P_Q = I_{\text{on}}^2 R_q \tag{25}\]

where \(I_{\text{on}}\) is the device conducting current. The body diode conduction loss is modeled with equation (3). The device switching loss is modeled as

\[
P_{\text{sw}} = K_q I_{\text{on}}^2 V_{\text{off}} f_{\text{sw}} \tag{26}\]

where \(f_{\text{sw}}\) is the switching frequency, \(I_{\text{on}}\) is the on-state device conducting current, and \(V_{\text{off}}\) is the off-state device blocking voltage. The body diode reverse-recovery loss is modeled...
switch is composed of six MOSFETs in parallel. The buck-
according to (6). To meet the worst-case current rating, each
switching losses are reduced by soft switching.

topology A shows better e
against the conventional boost converter, at a fixed 200 V
converter, particularly at light loads.

\[ L = \frac{v}{i} \]

parallel, with a switching frequency of 20 kHz. The optimized
stress is split between DCX primary and secondary sides;
therefore all switches can be realized with 600 V devices. Each
switch of the DCX is realized using 3 MOSFETs in parallel,
with a switching frequency of 30 kHz. As a consequence of
the increased power rating of the non-inverting buck-boost
module, each of its switches is realized using 8 MOSFETs in
parallel, with a switching frequency of 20 kHz. The optimized
inductor value is \( L = 63 \text{ mH} \).

As illustrated in Fig. 23, the composite converter B shows a
significant efficiency improvement over the conventional boost
converter at light load, although the heavy load efficiency
is worse. This is primarily a consequence of the increased
conduction loss of the non-inverting buck-boost module.

**TABLE IV**

<table>
<thead>
<tr>
<th>Converter Total Capacitor Power Rating Comparison with ( M_{\text{DCX}} = 4 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boost</td>
</tr>
<tr>
<td>---</td>
</tr>
<tr>
<td>Normalized total capacitor power ( P_{\text{Ch}} )</td>
</tr>
</tbody>
</table>

**TABLE V**

1200 V 100 A 2MB1100VA-120-50 IGBT Module Loss Model.

<table>
<thead>
<tr>
<th>IGBT</th>
<th>Conduction loss</th>
<th>( V_{\text{ce}} ) [V]</th>
<th>( R_{\text{f}} ) [mΩ]</th>
<th>0.75</th>
<th>14</th>
</tr>
</thead>
<tbody>
<tr>
<td>Turn-on loss</td>
<td>( k_{\text{on}} )</td>
<td>3.05 ( \times 10^{-8} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( a_{\text{on}} )</td>
<td>1.001</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( b_{\text{on}} )</td>
<td>0.84</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-off loss</td>
<td>( a_{\text{off}} )</td>
<td>0.75</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( b_{\text{off}} )</td>
<td>1.63</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**TABLE VI**

600 V 46 A FCH76N60NF Super-Junction MOSFET Loss Model.

<table>
<thead>
<tr>
<th>MOSFET</th>
<th>Conduction loss</th>
<th>( R_{\text{p}} ) [mΩ]</th>
<th>57.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching loss*</td>
<td>( a_{\text{on}} )</td>
<td>1.81</td>
<td></td>
</tr>
<tr>
<td>( b_{\text{on}} )</td>
<td>1.43</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Body diode</th>
<th>Conduction loss</th>
<th>( V_{\text{f}} ) [V]</th>
<th>0.6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reverse-recovery loss†</td>
<td>( a_{\text{off}} )</td>
<td>0.96</td>
<td></td>
</tr>
<tr>
<td>( b_{\text{off}} )</td>
<td>1.16</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\* \( E_{\text{on}} = K_{\text{d}} P_{\text{on}} V_{\text{in}}^2 \).

† \( E_{\text{off}} = K_{\text{d}} P_{\text{off}} V_{\text{in}}^2 \).

For these requirements, composite topology C requires
\( N_{\text{DCX}} = 2 \), and the voltage stresses of both the DCX and
the boost modules exceed 400 V. Therefore these modules are
designed with 1200 V 100 A IGBT devices. Consequently, the
boost module is designed for a switching frequency of 10 kHz,
with optimized inductance \( L = 108 \mu\text{H} \). The DCX module
operates with zero-voltage switching at 30 kHz. The composite
converter C efficiency curve in Fig. 23 achieves a substantial
efficiency improvement over the conventional boost approach,
in spite of the need to employ 1200 V Si IGBTs.

Composite topology D allows all device voltage stresses to
be limited to 400 V, and hence 600 V devices can be employed
in all modules. Each switch in the composite converter D is
composed of five MOSFET dies in parallel, except that the
DCX secondary side switches utilize two MOSFET dies in
parallel. Both buck and boost modules operate at switching
frequencies of 20 kHz with \( L = 72 \mu\text{H} \). The DCX module
operates at a switching frequency of 30 kHz. In Fig. 23, the
predicted efficiency curve of composite converter D achieves
the best efficiency among all composite converter architectures,
with a loss reduction of approximately 50% at medium load.

A scaled-down 10 kW composite converter D prototype was
built and reported in [24], with detailed design parameters.
documented. A peak efficiency of 98.7% was measured at approximately 210 V input, 650 V output with 5 kW output power, and the measured efficiency exceeded 97% over a wide operation range.

In [26], a 30 kW composite converter prototype was reported, including a calibrated loss model and detailed design optimization procedure. Figure 24 shows the measured efficiency at $V_{\text{battery}} = 210$ V and $V_{\text{bus}} = 650$ V, from [26]. A peak efficiency of 98.4% was reported, and the measured efficiency agrees well with theoretical loss model.

In this section, designs based on the prior-art SAZZ, coupled-inductor, and three-level approaches are modeled using comparable physical device parameters, and their efficiencies are compared with the conventional boost approach as well as with the proposed composite D converter approach. For the 30 kW application defined above, the Z-source inverter requires 2100 V devices. It is concluded that the Z-source inverter is not a competitive solution for this application.

Figure 25 plots the efficiency vs. power for the different approaches at a fixed 200 V input and 650 V output.

The SAZZ approach efficiency curve is generated by assuming the soft-switching efficiency is $\eta_{ss} = 50\%$. This is an optimistic assumption, since the previously reported $\eta_{ss}$ was less than 40% [11], and the increased losses in the added magnetics and semiconductor devices are ignored. However, even with these idealized assumptions, the overall system efficiency improvement is modest: approximately 0.7% at medium load, as compared against the conventional boost approach.

To compare the performance of the coupled inductor approach, a bi-directional coupled-inductor boost converter is designed. Because the output bus voltage is 800 V, a 1200 V IGBT is required. However, each phase is only required to carry half of the total current, therefore 1200 V 100 A devices are used, with device parameters documented in Table V. The magnetics are optimized so that the total magnetic core volume is the same as in the conventional boost converter. The calculated optimum inductance is $135 \mu H$ at 10 kHz switching frequency. The modeled coupled inductor approach efficiency is compared in Fig. 25. This approach improves the medium to heavy load efficiency by approximately 1.2% relative to the conventional approach. Even with additional transformer loss, the total magnetics loss is nonetheless slightly reduced. However, the predicted efficiency is still much lower than the results reported in [17]. This is because in [17], operating voltages are lower, and 600 V MOSFETs with SiC Schottky diode were therefore used. The switching frequency is increased to 45 kHz, and the magnetics can be designed with ferrite cores and substantially reduced magnetics loss. For the operating voltages considered here, silicon 1200 V IGBTs exhibit much higher switching losses, the switching frequency is limited to 10 kHz, and the magnetics loss is substantially increased. It can be concluded that the coupled inductor approach is more advantageous in relatively low voltage applications. These advantages could extend to higher voltages based on emerging higher voltage SiC MOSFET devices.

In the three-level converter the device voltage stress is reduced by one half. Hence, 600 V MOSFETs are used in the three-level converter design. The loss model is summarized in Table VI. To reduce the device on-resistance and increase current capability, several MOSFET dies are connected in parallel for each switch. Twelve MOSFET dies per switch are found to yield a good tradeoff between conduction and switching losses. For this design, the switching frequency is 20 kHz, and the inductance is reduced to $85 \mu H$.

As shown in Fig. 25, the efficiency of the three-level converter is substantially improved relative to the conventional boost approach. The ability to employ 600 V MOSFETs enables lower conduction and switching losses compared to IGBTs. The magnetics loss is also further reduced because of the higher switching frequency and reduced volt-seconds applied to the inductor by the three-level switching waveform. Compared with the conventional boost, the three-level converter efficiency at medium to heavy load is improved by approximately 1.8% with 600 V MOSFETs, and the loss is reduced by a factor of approximately two. It can be observed
D. Comparison of average efficiency over standard driving test cycles

Improvement of the efficiency of indirect power conversion, via the composite converter approach, can lead to significant mission-related performance improvements. In the electrified vehicle application, the composite converter approach can lead to substantial improvements in efficiency and total power loss under actual driving conditions. Especially noteworthy is the improvement in low-power efficiency and its influence on the total loss. In this section, the impact of the composite converter approach is estimated for three standard US EPA drive cycles: UDDS (city driving), HWFET (highway driving), and US06 (aggressive driving). Significant and non-incremental improvements in total loss and in converter quality factor $Q$ are predicted; these could lead to improvements in MPGe, in cooling system size and weight, and in system cost.

Simulation of the converter efficiency and loss over a given driving cycle requires assumptions regarding the vehicle, motor, and system architecture. A typical mid-size sedan is modeled here. A 60 kW 16-pole permanent magnet synchronous motor (PMSM) is modeled, based on experimental data extracted from the Toyota Prius 2010 in [7]. The motor is coupled to the vehicle with a gear ratio of 8.62. In the simulation, the actual voltage profile is employed, while the current is scaled according to the motor rated power, to match the 30 kW DC-DC converter model of the previous sections. The space vector pulse-width modulation (SVPWM) scheme [49] is used in the inverter. The simple constant torque-angle ($90^\circ$) control [50] is used, except that at high speed field weakening is applied to limit the dc bus voltage to no greater than 800 V. It is assumed that the battery has a constant voltage of 200 V, and the DC-DC converter is controlled so that the DC-DC converter output voltage is equal to the inverter peak line voltage, except when the peak line voltage is smaller than the 200 V battery voltage. Since all converter modules are capable of bi-directional power flow, 100% regenerative braking is assumed.

Figures 26–28 show the bus voltage and output power probability distributions for the three simulated driving cycles. Also shown are one-dimensional probability density functions (PDF) for the bus voltage and output power. In the UDDS driving cycle, the bus voltage is mostly confined to the range 200 V to 300 V, with output power less than 10% of maximum, due to the low-speed urban driving pattern. In the HWFET driving cycle, bus voltage is mostly in the range 400 V to 600 V, with output power approximately 10%; this corresponds to cruising at relatively high speed. In the US06 driving cycle, the bus voltage is mostly in the range 600 V to 800 V, with output power approximately 20%, although a peak power exceeding 70% is recorded, and significant trajectories of proportional bus voltage and output power are caused by the many accelerations and decelerations of the US06 cycle.

Table VII documents the simulated drive cycle converter quality factor $Q$ for the different converter approaches. The loss and power throughput are integrated over each drive cycle to compute an average $Q$. In all three different driving profiles, both the three-level converter and composite converter D show significant efficiency improvements over the conventional boost converter. In the UDDS urban driving test, the converter quality factor of composite converter D is almost twice of that of conventional boost converter, which means the power throughput per unit loss of composite converter D is almost doubled. In the HWFET highway driving test, the converter quality factor of composite converter D is increased by more than a factor of four relative to the conventional boost converter. In the

\[ Q = \frac{\int |P_{\text{out}}| \, dt}{\int P_{\text{loss}} \, dt} \]  

(27)
The coupled inductor approach uses four silicon 1200 V 100 A devices, if the extra auxiliary switch elements are ignored. The SAZZ approach will use roughly the same semiconductor capacitor energy rating. In terms of semiconductor devices, the total magnetic core volume is designed to be the same as in the conventional boost approach.

As noted previously, the capacitor rms current rating typically is the dominant constraint limiting the size of the capacitors in electrified vehicle applications. The total capacitor power rating \((I_{\text{cap}, \text{rms}} - \text{max}) V_{\text{cap}, \text{max}}\) summed over all capacitors) is a good measure of the volume and cost of the capacitor module. The power ratings listed in Table VIII include details such as inductor current ripple and DCX non-trapezoidal transformer current waveforms, which cause the data in Table VIII to be somewhat higher than the idealized data of Table IV. In Table VIII, the total capacitor energy rating is calculated, based on designs that result in ±5 V worst-case output voltage ripple. The snubber capacitor of the SAZZ approach is ignored. Therefore the SAZZ approach requires roughly the same capacitor power and energy rating as the conventional boost converter. The coupled inductor approach is basically a two-phase interleaved converter, and therefore the capacitor power rating is reduced by 47%, while the energy rating is only a quarter of that in the conventional boost approach. The three-level converter requires a flying capacitor which carries a large rms current at a voltage rated half of the output bus voltage. For the 30 kW design considered here, a 200 Arms 400 V capacitor is required. This may substantially increase the system size and cost. Relative to the conventional boost, the capacitor power rating is increased by 91%, while the energy rating is increased by 49%, even though it switches at a higher frequency. In contrast, although the composite converter D increases the number of capacitors required, the capacitor voltage rating is much reduced. Further, because the indirect power path is processed with a DCX module having a quasi-square wave converter with very small current ripple, the capacitor rms current rating and voltage ripple can both be reduced. This leads to a 40% reduction in the total capacitor power rating. The composite converter D also achieves an 85% reduction in the total capacitor energy rating.

In a typical electrified drive train system, the film capacitor modules exhibit higher volume and cost than the magnetics. For example, the capacitor module of the Prius 2004 has volume larger than 6 L, while the remainder of the converter module has volume of 1.1 L [6]. Therefore, although the three-level converter approach achieves excellent efficiency, it leads to significantly increased system size and cost because of the large flying capacitor. Other multi-level approaches such as [51] suffer from this issue as well. It should be noted that US06 driving test, the converter quality factor is increased by more than a factor of three as well. The three-level converter out-performs composite D converter in the low speed UDDS driving test, while the composite converter D shows higher converter quality factor in high speed HWFET and US06 driving tests. However, as illustrated in the following section, the three-level converter requires much larger capacitor modules, which are challenging to implement and can significantly increase the system size and cost.

### Converter size comparison

Table VIII compares composite converter D with prior approaches in terms of total semiconductor devices, total magnetics core volume, total capacitor power rating, and total capacitor energy rating. In terms of semiconductor devices, the boost converter uses two silicon 1200 V 200 A IGBT modules. The SAZZ approach will use roughly the same semiconductor devices, if the extra auxiliary switch elements are ignored. The coupled inductor approach uses four silicon 1200 V 100 A IGBT modules, and is similar to the conventional approach in total device area. Both the three-level converter and composite converter D use silicon 600 V 46 A MOSFETs, and both employ a total of 48 MOSFET die. The semiconductor utilization in all approaches is similar.

Regarding the total magnetic core volume, the total core volume of the SAZZ approach can be taken to be the same as in the conventional boost approach, if the magnetics of the active snubber is ignored. The coupled inductor approach basically takes the conventional boost inductor, and splits it into one smaller inductor and one transformer. Therefore the total magnetics size is unchanged. Because the three-level converter reduces the applied inductor volt-seconds, the inductor size is reduced by 65%. The composite converter D total magnetic core volume is designed to be the same as in the conventional boost approach.

As noted previously, the capacitor rms current rating typically is the dominant constraint limiting the size of the capacitors in electrified vehicle applications. The total capacitor power rating \((I_{\text{cap}, \text{rms}} - \text{max}) V_{\text{cap}, \text{max}}\) summed over all capacitors) is a good measure of the volume and cost of the capacitor module. The power ratings listed in Table VIII include details such as inductor current ripple and DCX non-trapezoidal transformer current waveforms, which cause the data in Table VIII to be somewhat higher than the idealized data of Table IV. In Table VIII, the total capacitor energy rating is also calculated, based on designs that result in ±5 V worst-case output voltage ripple. The snubber capacitor of the SAZZ approach is ignored. Therefore the SAZZ approach requires roughly the same capacitor power and energy rating as the conventional boost converter. The coupled inductor approach is basically a two-phase interleaved converter, and therefore the capacitor power rating is reduced by 47%, while the energy rating is only a quarter of that in the conventional boost approach. The three-level converter requires a flying capacitor which carries a large rms current at a voltage rated half of the output bus voltage. For the 30 kW design considered here, a 200 Arms 400 V capacitor is required. This may substantially increase the system size and cost. Relative to the conventional boost, the capacitor power rating is increased by 91%, while the energy rating is increased by 49%, even though it switches at a higher frequency. In contrast, although the composite converter D increases the number of capacitors required, the capacitor voltage rating is much reduced. Further, because the indirect power path is processed with a DCX module having a quasi-square wave converter with very small current ripple, the capacitor rms current rating and voltage ripple can both be reduced. This leads to a 40% reduction in the total capacitor power rating. The composite converter D also achieves an 85% reduction in the total capacitor energy rating.

In a typical electrified drive train system, the film capacitor modules exhibit higher volume and cost than the magnetics. For example, the capacitor module of the Prius 2004 has volume larger than 6 L, while the remainder of the converter module has volume of 1.1 L [6]. Therefore, although the three-level converter approach achieves excellent efficiency, it leads to significantly increased system size and cost because of the large flying capacitor. Other multi-level approaches such as [51] suffer from this issue as well. It should be noted that

### TABLE VIII

<table>
<thead>
<tr>
<th></th>
<th>Boost</th>
<th>SAZZ</th>
<th>Coupled inductor</th>
<th>Three-level</th>
<th>Composite D</th>
</tr>
</thead>
<tbody>
<tr>
<td>UDDS</td>
<td>38.6</td>
<td>44.9</td>
<td>62.4</td>
<td>117.5</td>
<td>74.5</td>
</tr>
<tr>
<td>HWFET</td>
<td>17.5</td>
<td>20.2</td>
<td>35.5</td>
<td>71.4</td>
<td>75.2</td>
</tr>
<tr>
<td>US06</td>
<td>21.9</td>
<td>26.4</td>
<td>34.0</td>
<td>57.7</td>
<td>67.1</td>
</tr>
</tbody>
</table>

Fig. 28. \(V_{\text{bus}}\) and normalized \(|P_{\text{out}}|\) probability distribution in simulated US06 driving cycle.
 deployment of more advanced device technologies, such as GaN or SiC transistors [52] with higher switching frequencies, does not address the issue of capacitor rms current rating, and therefore would not lead to reduced capacitor size and cost. Hence the composite converter approach achieves a combination of substantially reduced loss and substantially reduced capacitor size and cost. Non-incremental improvements can be achieved, relative not only to the conventional boost converter but also relative to other candidate approaches such as the three-level, SAZZ, and coupled-inductor circuits.

VI. CONCLUSIONS

The electrified automotive powertrain is a thermally limited system. To address the fact that a limited amount of loss can be tolerated by a given thermal management system, the converter quality factor $Q = P_{\text{out}}/P_{\text{loss}}$ is introduced here as a metric of converter performance. Systems having higher average $Q$ over a driving cycle not only achieve improved MPGe, but also can achieve higher system power density, and/or the size and cost of the thermal management system can be reduced. The powertrain system must be rated to handle the maximum power, at least for a limited time; nonetheless, the efficiency of the powertrain dc-dc converter at medium to light load conditions is critical to $Q$ in standard driving cycle tests.

In this work, existing boost converter technologies are reviewed and their performances are compared in a standardized manner with paper designs using realistic loss models. Techniques including the soft-switching approach and the coupled inductor approach do not address reduction of all dominant loss mechanisms, and hence they provide only incremental efficiency improvements. The three-level converter approach does show promising efficiency improvements on paper, but the extra flying capacitor conducts substantial rms current that leads to significant increases in the system size and cost.

To overcome the limitations of the previous approaches, a composite boost converter is proposed. This approach employs a dc transformer module to process most of the indirect power in a more efficient way, and combines several smaller converter modules into a composite system. Each module processes a fraction of the total system power, with higher efficiency. At a given operating point, one or more of the converter modules operate either in shut down or in pass through mode, reducing the ac power loss. Several composite converter topologies are explored in this work. In this specific application of an automotive powertrain system, the composite converter topology D achieves a superior efficiency improvement over the conventional boost converter. Standard driving cycle simulations predict that composite converter D approximately doubles the converter quality factor $Q$ in the UDDS (urban) driving cycle, and the converter quality factor is increased by more than a factor of four in the HWFET (highway) driving cycle. The total system capacitor power rating is reduced by a factor of more than 40%, while the total capacitor energy rating is reduced by almost 85%. This suggests that the proposed composite boost converter approach is a viable and promising future technology to replace the conventional boost converter in the automotive electrified powertrain application. Several prototypes [24]–[26] have been built to demonstrate this technology, and its feasibility has been well validated.

As summarized in Table III, the total volt-amperes applied to the semiconductor devices of the composite D approach are approximately the same as in the conventional boost converter, and hence one would expect the total power semiconductor area to be similar. However, the Composite D approach requires a larger number of (smaller) transistors. Since the power semiconductors of electrified vehicles are normally multiple parallel-connected dies that are co-packaged in a multichip power semiconductor module, the Composite D approach simply requires more complex interconnections. There is much current research in power semiconductor packaging, including topics such as three-dimensional interconnects. This paper shows that this greater complexity can lead to substantial benefits of non-incremental reductions in system loss and in film capacitor size.

ACKNOWLEDGEMENT

The information, data, or work presented herein was funded in part by the Office of Energy Efficiency and Renewable Energy (EERE), U.S. Department of Energy, under Award Number DE-EE0006921.

REFERENCES


| TABLE VIII | Converter Size Comparison |
|---|---|---|---|
| **Semiconductor devices** | **Boost / SAZZ** | **Coupled inductor** | **Three-level** | **Composite D** |
| Total magnetics core volume | 360 cm$^3$ | 360 cm$^3$ | 195 cm$^3$ | 360 cm$^3$ |
| Total capacitor power rating | 85 kVA | 45 kVA | 160 kVA | 51 kVA |
| Total capacitor energy rating* | 162 J | 42 J | 242 J | 25 J |

*Assume worst-case ±5 V output voltage ripple.


Hua Chen received his B.Eng. (2010) degree from The Chinese University of Hong Kong. From spring 2012, he is studying toward Ph.D. degree at the Department of Electrical, Computer and Energy Engineering in the University of Colorado at Boulder. His research interests include high efficiency DC-DC converter for electric vehicles and power management IC design.

Hyokjin Kim received the B.Sc. and M.Sc. degrees in electrical engineering from Hongik University, Korea, in 2009 and 2011, respectively. He is currently working toward his Ph.D. degree at the University of Colorado, Boulder, CO, USA. His research interests include converter design, digital control, modeling, energy harvesting.

Robert Erickson earned the B.S. (1978), M.S. (1980), and Ph.D. (1982) degrees from the California Institute of Technology. Since 1982, he has been on the faculty of the ECEE Department at the University of Colorado-Boulder, where he served as Chair in 2002–2006 and 2014–2015. He and Prof. Maksimovic co-direct the Colorado Power Electronics Center. His research interests include electric vehicle power electronics (charger and drive train power conversion), grid interface of solar and wind power systems, low harmonic rectification, resonant power conversion, and power electronics modeling and control. He is a Fellow of the IEEE, a Fellow of the UC-B/NREL Renewable and Sustainable Energy Institute, and an author of the textbook Fundamentals of Power Electronics.

Dragan Maksimovic (M’89–SM’04–F’15) received the B.S. and M.S. degrees in electrical engineering from the University of Belgrade, Serbia (Yugoslavia), in 1984 and 1986, respectively, and the Ph.D. degree from the California Institute of Technology, Pasadena, in 1989. From 1989 to 1992, he was with the University of Belgrade. Since 1992, he has been with the Department of Electrical, Computer and Energy Engineering, University of Colorado, Boulder, where he is currently a Professor and Co-Director of the Colorado Power Electronics Center (CoPEC). His current research interests include power electronics for renewable energy sources and energy efficiency, high frequency power conversion using wide bandgap semiconductors, digital control of switched-mode power converters, as well as analog, digital and mixed-signal integrated circuits for power management applications.

Prof. Maksimovic has co-authored over 250 publications and the textbook Fundamentals of Power Electronics. He received the 1997 NSF CAREER Award, the IEEE PELS Transactions Prize Paper Award in 1997, the IEEE PELS Prize Letter Awards in 2009 and 2010, the University of Colorado Inventor of the Year Award in 2006, the IEEE PELS Modeling and Control Technical Achievement Award for 2012, the Holland Excellence in Teaching Awards in 2004 and 2011, the Charles Hutchinson Memorial Teaching Award for 2012, and the 2013 Boulder Faculty Assembly Excellence in Teaching Award.