Microscale Power Conversion (MPC)

Quarterly Review Telecon
February 28, 2014
University of Colorado, Boulder and TriQuint Semiconductor
Co-PIs: Zoya Popovic, Dragan Maksimovic

UC-Boulder: Dr. David Sardin, Dr. Miguel Rodriguez, Dr. Tibault Rebeyrand, Andrew Zai, Scott Schafer, Yuanzhe Zhang, Dongxue Li, Mike Litchfield, Mike Coffey
TriQuint technical support: Dr. Chuck Campbell, John Hitt; PM: Maureen Kalinski
Overview

1. MMI C RFPA summary, Run 2
2. MMI C iDSM2 summary, Run 2
3. MMI C RF-DSM summary, Run 2
4. Low-frequency drain transistor/PA model
5. Signal considerations
6. Results from new MPC-inspired concepts
MMIC PA Design: 0.15um GaN MPC Run#2

Class-E PA
10W

Class-AB PA

Class-AB
10GHz, 4W
Driver 20GHz
HI-PA

10GHz +
20GHz PA
HI-integrated

PA +
Cascode Modulator

iDSM2 Bootstrap
10W, Gsat=20dB

iDSM2 Pull-up

Test structures

iDSM2 Active pull-up

Isolated Outphasing w/recycling

iDSM2 Active pull-up +level-shifter

7/16/2014
## Circuit label | Circuit type | Main parameters | Goals |
<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>Ckt1-A</td>
<td>Class-E PA</td>
<td>&gt;10W, PAE=60%, 21dB (2s) <em>Odd mode oscillation</em></td>
<td>High-gain, high eff, power spec</td>
</tr>
<tr>
<td>Ckt2-B</td>
<td>Class-AB PA</td>
<td>&gt;12W, PAE=55%, Gsat=23dB</td>
<td>High-gain, high eff, power spec, lower drain impedance</td>
</tr>
<tr>
<td>Ckt3-C</td>
<td>Bootstrap</td>
<td><em>100 MHz switching frequency, 78.5% efficiency</em></td>
<td>Alternative modulator (iDSM) topology: <em>functional, but inferior efficiency</em></td>
</tr>
<tr>
<td>Ckt4-D</td>
<td>Class-AB 10GHz Driver 20GHz</td>
<td>4W, PAE=60% (preliminary) 1W, PAE=40%</td>
<td>Test circuits for Ckt7; Harmonic injection</td>
</tr>
<tr>
<td>Ckt5-E</td>
<td>5mm PA</td>
<td>10W, PAE=60%, Gsat=20dB 15W, 10GHz, G=23dB, PAE&gt;60%</td>
<td>High-gain, high eff, power spec</td>
</tr>
<tr>
<td>Ckt6-F</td>
<td>Pull up</td>
<td><em>Not tested yet</em></td>
<td>Alternative integrated DSM topology</td>
</tr>
<tr>
<td>Ckt7-G</td>
<td>10GHz + 20GHz PA integrated</td>
<td>4W, PAE&gt;60%, Gsat=9dB 4W, 10.6GHz, PAE&gt;70%</td>
<td>Harmonic injection for high efficiency and high linearity</td>
</tr>
</tbody>
</table>

*New integrated modulator iDSM2 test results highlighted*  
*New RFPA test results highlighted*
## New integrated modulator iDSM2 test results highlighted

<table>
<thead>
<tr>
<th>Circuit label</th>
<th>Circuit type</th>
<th>Main parameters</th>
<th>Goals</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ckt8-H</td>
<td>Test Structures</td>
<td>calibration kit and single transistors (10x90, 8x40), Test PA for Ckt11</td>
<td>Modelithics model validation, PA validation for Ckt11</td>
</tr>
<tr>
<td>Ckt9-I</td>
<td>Modulator (without lvl shifter)</td>
<td>&gt;5W, &gt;90%, 100 MHz Tests at 10-200 MHz switching frequency</td>
<td>High-efficiency 100 MHz iDSM2, feasibility of integration with PA</td>
</tr>
<tr>
<td>Ckt10-J</td>
<td>PA + Cascode Modulator</td>
<td>3W PA with integrated cascode for 500MHz bandwidth <strong>Compressed Gain = 19-20 dB</strong> <strong>PAE &gt; 70% for 20 MHz&lt;f&lt;300 MHz</strong></td>
<td>Begin integration of power amplifier and DSM</td>
</tr>
<tr>
<td>Ckt11-K</td>
<td>Outphasing</td>
<td>5W PA, PAE=60% <strong>Not tested yet, hybrid test finished</strong></td>
<td>Isolated outphasing PA with PA rectifier</td>
</tr>
<tr>
<td>Ckt12-L</td>
<td>Modulator (with lvl shifter)</td>
<td>&gt;5W, 83.5%, 100 MHz switching frequency</td>
<td>Modulator with integrated level shifter: test ability to drive with logic-level signals</td>
</tr>
</tbody>
</table>
1. MMIC PAs designed for Vdd variation

Run 1, 10W, very nonlinear

Run 2, >10W, more linear
1. MMIC PA example results
State-of-the-art, X-band GaN PAs

MPC PAs


2. DSM MMIC designs

Summary of iDSM2 test results

Circuit I: Modified active pull-up MMIC switcher iDSM2.3 MMIC
- Successfully tested at 10-200 MHz frequency
- Best efficiency (>90%) results at >5W

Circuit L: Level shifter MMIC switcher iDSM2.4 (Circuit L)
- Tested at 100 MHz switching frequency, with logic-level inputs
- Functional level-shift and gate drive circuitry
- Efficiency lower than in Circuit I, but improvements should be possible with better models

Circuit C: Bootstrapped iDSM2.1 MMIC switcher
- Functional, but efficiency is lower

We are currently designing integrated switchers in TQS PDK#2 (TA1) based on Circuit I and Circuit L configurations
Integrated MMIC switcher (iDSM2)

Circuit I: Modified active pull-up iDSM2.3 MMIC

VinLs  VinHs  Vdd  SW

20-pin 4x4 mm QFN package
Integrated 100 MHz iDSM2.3 test setup

- MMIC driver/bias consumption at 100 MHz switching frequency: 0.1 W
- Vin supply: 20 V
- Switch duty cycle resolution: 125 ps

Diagram showing
- FPGA to LVDS Receiver
- LVDS Receiver to PA
- Bias tee to VinHs
- Bias tee to VinLs
- -V_GHbias, -V_SHbias, -V_GLbias, -V_SLbias
- 47 nH/39 nH/22 nH Coilcraft aircore 1812SMS-

47 nH/39 nH/22 nH
Coilcraft aircore
1812SMS-
Waveforms: Modified active pull up iDSM2.3 (Circuit I)

\[ V_{\text{in}HS} \]

\[ V_{\text{in}LS} \]

\[ V_{\text{sw}} \]

\[ D = 0.75 \]

\[ 2.5 \text{ ns/div} \]

\[ V_{\text{out}} = 14 \text{ V}, \quad P_{\text{out}} = 2.2 \text{ W}, \quad \eta = 91.0 \% \]
Efficiency & loss breakdown: iDSM2.3 (Circuit I)

Inductor $L = 47 \text{ nH}$

<table>
<thead>
<tr>
<th>Loss breakdown [mW]</th>
<th>Inductor DC, 0.5, 0%</th>
<th>Inductor AC, 15.9, 4%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching</td>
<td>274.7, 59%</td>
<td></td>
</tr>
<tr>
<td>HEMT cond.,</td>
<td>150.6, 34%</td>
<td></td>
</tr>
</tbody>
</table>

Inductor $L = 39 \text{ nH}$

<table>
<thead>
<tr>
<th>Loss breakdown [mW]</th>
<th>Inductor DC, 0.5, 0%</th>
<th>Inductor AC, 19.9, 4%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching</td>
<td>274.7, 59%</td>
<td></td>
</tr>
<tr>
<td>HEMT cond.,</td>
<td>169.4, 37%</td>
<td></td>
</tr>
</tbody>
</table>

Inductor $L = 22 \text{ nH}$

<table>
<thead>
<tr>
<th>Loss breakdown [mW]</th>
<th>Inductor DC, 0.5, 0%</th>
<th>Inductor AC, 25.8, 5%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching</td>
<td>218.5, 42%</td>
<td></td>
</tr>
<tr>
<td>HEMT cond.,</td>
<td>271.8, 53%</td>
<td></td>
</tr>
</tbody>
</table>
200 MHz iDSM2.3 test (Circuit I)

Inductor \( L = 22 \, \text{nH} \)

\[
\begin{align*}
V_{out} &= 14 \, \text{V}, \quad P_{out} = 2.2 \, \text{W}, \quad \eta = 77.7 \% \\
V_{out} &= 14 \, \text{V}, \quad P_{out} = 5.0 \, \text{W}, \quad \eta = 82.0 \%
\end{align*}
\]
• Operating conditions: $V_{\text{in}}=20\ \text{V}$, $P_{\text{out}}=5\ \text{W}$, $D=0.75$

<table>
<thead>
<tr>
<th>$f$ [MHz]</th>
<th>$L$ [nH]</th>
<th>Coilcraft Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>538</td>
<td>132-20SMJLB</td>
</tr>
<tr>
<td>40</td>
<td>90</td>
<td>132-09SMJLT</td>
</tr>
<tr>
<td>100</td>
<td>47</td>
<td>1812SMS-47NJLB</td>
</tr>
<tr>
<td>200</td>
<td>22</td>
<td>1812SMS-22NJLB</td>
</tr>
</tbody>
</table>
Integrated MMIC switcher iDSM2.1 (Circuit C)

Circuit C:
Bootstrapped iDSM2.1 MMIC

20-pin 4x4 mm QFN package
iDSM2.1 Circuit C test results

- Test setup similar to iDSM2.3 (Circuit I) shown before
- Efficiency lower than in Circuit I
- Testing in progress, but the approach will most likely not be pursued further in the next DSM designs

Inductor $L = 27 \text{ nH (1111SQ series)}$

$V_{\text{out}} = 10 \text{ V, } P_{\text{out}} = 2.5 \text{ W, } \eta = 78.5 \%$

$D = 0.5$  2.5 ns/div

20 V
Level shifter integrated MMIC switcher iDSM2.4 (Circuit L)

Circuit I (Modified active pull-up iDSM2.3)

Circuit L: Level shifter integrated modified active pull-up iDSM2.4

High side level shifter (Low side is identical, not shown for simplicity)

From low side level shifter

0/3.3 V logic level input

2.1mm

2.8mm

24-pin 5x5 mm QFN package

Vdd

Vdd1HS

Vdd2HS

VcHS

Vss1HS

Vss2HS

Vss3HS

VinLS

Vdd1LS

Vdd2LS

VcLS

Vss1LS

Vss2LS

Vss3LS

SW

SW

SW

Vdd
• Logic-level inputs: very easy to interface to the FPGA control circuitry
• Integrated MMIC level shifter and driver consumption at 100 MHz switching frequency: ~0.36 W
• Vin supply: 20 V
• Switch duty cycle resolution: 125 ps
Inductor $L = 47 \text{ nH}$

- $D = 0.5$
  - $V_{out} = 10 \text{ V}$, $P_{out} = 1.9 \text{ W}$, $\eta = 68.5\%$

- $D = 0.75$
  - $V_{out} = 15 \text{ V}$, $P_{out} = 5.8 \text{ W}$, $\eta = 83.5\%$

EG0490L: Level shifter integrated modified Active Pull-Up iDSM2.4 (power stage only)

- The level shifter is functional
- Design could be improved based on better simulation models
DSM4 : VHF/UHF RF PA approach

- AC coupled Cascode amplifier topology with 2 biasing configurations

**Regular**

Max $V_{dd} = 25\, \text{V}$
(Process limitation)

$P_{out\_average} = 36\, \text{dBm} @ V_{dd} = 20\, \text{V}$

**Self biased**

Allows higher $V_{dd}$
(twice nominal)

Higher output power but choke parasitic limitation
DSM4: VHF/UHF, 15MHz – 500MHz

- Bandwidth: 15 MHz to 500 MHz
- Cutoff frequency of 15 MHz is related to the choke inductor value
- Scope based measurement is ongoing for frequency from DC to 15 MHz

50 Ω based Small Signal measurement

\[ |S_{21}| = 24 \text{ dB} \]

\[ |S_{11}| < -8.5 \text{ dB} \]
Compressed Gain = 19-20 dB

PAE > 70% for 20 MHz < f < 300 MHz

$V_{dd}$ was set to 30 V for safety (drain bias point of the bottom transistor may shift during power sweep)

<table>
<thead>
<tr>
<th></th>
<th>$V_{dd}$ (V)</th>
<th>Bandwidth (MHz)</th>
<th>Gain @ max Pout</th>
<th>Pout dBm (av)</th>
<th>PAE (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Regular</td>
<td>20</td>
<td>25 to 500</td>
<td>19</td>
<td>36</td>
<td>51 to 85</td>
</tr>
<tr>
<td>Self biased</td>
<td>30</td>
<td>15 to 500</td>
<td>20</td>
<td>40</td>
<td>39 to 75</td>
</tr>
</tbody>
</table>
DSM4 : VHF/UHF RF PA approach

- Extend bandwidth at lower frequencies
- Investigate DC coupled structure
- Scope based measurement required
- Input DC gate voltage provided from the AWG
- Problem : Drain biasing network

  - Choke inductor cannot be used due to nonphysical value
  - Solution : Active or resistive bias tee

Active Bias Tee operating down to DC

4. Low-Frequency Drain Modeling (co-design)

• Goal:
  • Describe impedance variations of transistor from 1MHz – 500MHz
    • Variations from DC bias point
    • Variations from modulation
    • Variations from RF power

• This will allow:
  • Determine impedance variation of full power amplifier
  • Operation points for optimal baseband to RF conversion
  • For already designed PAs: Design optimal supply modulation trajectory by limiting highly dynamic load variations
  • For future PA designs: Minimize drain impedance variation to reduce requirements of SM (to work under dynamic loads) while keeping high RF efficiency
  • Predict and ensure stability of transmitter (RFPA + SM)
Transistor drain impedance

- Inject power simultaneously at gate and drain
  - Gate: RF at 10GHz
  - Drain: LF at 10MHz
Drain Impedance Variations (Simulation) versus DC Bias Point

- Derivative of IV curves gives static drain impedance

\[
\frac{\partial I_d}{\partial V_d} \bigg|_{V_g} = \frac{1}{\text{Re}[Z_d]}
\]
Drain Impedance Variations (Simulation) versus Low frequency Power

- 10x90um Device
- Bias point: $V_G = -2.5V$, $V_D = 20V$
- RF: 10GHz, LF: 10MHz

- Red line: 24dBm LF power
- Blue line: 16dBm RF Input power
Drain Impedance Variations (Simulation) versus Low Frequency power

- $Z_D$ variations can be explained by time average of static impedance found from IV curves
  - Example: Biased at $V_D=7.5V$, sinusoidal variations at impedance will cause time average to drop faster than when biased at $V_D=20V$
Drain Impedance Variations (Simulation) versus RF Input Power

- 10x90um Device
- Bias point: $V_G = -2.5V$, $V_D = 20V$
- RF: 10GHz, LF: 10MHz
- Red line: 24dBm LF power
- Blue line: 16dBm RF Input power
• Observations of $Z_D$ (10MHz):
  • Large $Z_D$ variation around RF saturation - Varies from 200 to 50ohm
  • Reactance is small (as expected; bias line capacitance will dominate in RFPA)
Frequency variation can be roughly modeled as a RC parallel circuit

- 10x90um Device
- Bias point: \( V_G = -2.5V \), \( V_D = 20V \)
- RF: 10GHz
- 24dBm LF power
- 16dBm RF Input power

Can explain transistor \( Z_D \) variations over DC bias, LF drain power and frequency

Working on explaining \( Z_D \) variations with RF input power – Measurements!

- Multi-frequency setup to measure LF + RF parameters on probe station
- Drain bias tee designed for LF modulation with RF output
5. Signal considerations

Comparison of Drain Efficiency for Class-A and Class-B with and without Supply Modulation

Class-A

\[ \eta = \frac{2A^2}{I_{\text{max}}^2} \quad (\text{static bias}) \]

\[ \eta = \frac{A}{I_{\text{max}}} \quad (\text{dynamic bias}) \]

Class-B

\[ \eta = \frac{A\pi}{4I_{\text{max}}} \quad (\text{static bias}) \]

\[ \eta = \frac{V_{\text{max}} - V_k}{2\pi} \frac{A}{A + \frac{V_k I_{\text{max}}}{\pi}} \quad (\text{dynamic bias}) \]
Gaussian Envelope for LFM pulses

Instantaneous Drain Efficiency of a Gaussian Pulse for Various Modes of Operation

<table>
<thead>
<tr>
<th>Mode of Operation</th>
<th>Average Efficiency</th>
<th>Power Needed for Pout = 10 W</th>
</tr>
</thead>
<tbody>
<tr>
<td>Class-A (Static)</td>
<td>14.1%</td>
<td>70.4W</td>
</tr>
<tr>
<td>Class-B (Static)</td>
<td>31.4%</td>
<td>31.8 W</td>
</tr>
<tr>
<td>Class-A (Dynamic)</td>
<td>20.0%</td>
<td>50.0 W</td>
</tr>
<tr>
<td>Class-B (Dynamic)</td>
<td>48.9%</td>
<td>20.4 W</td>
</tr>
</tbody>
</table>
Architecture for Amplitude Modulation Radar

![Diagram of AM Waveforms and Drive Control Resonant Modulator](image)

- **Nominal operation**
- **AM Waveforms**
- **Temporary increase in peak power**
- **Increased operating power**
- **Nominal operating power**

**Mode 1**

**Mode 2**

**Mode 3**

**Mode 1**

Drive Control

Resonant Modulator

Driver Amp

Carrier Amp

Peaking Amp

MMIC PA

Efficiency vs. Drive Voltage

- Mode 1
- Mode 2
- Mode 3
Simulations with Doherty MMIC from Run 1

Constant Supply
Modulated Supply

Constant Supply
Modulated Supply

DC Power (W)

Dissipated Power (W)

RF Output Power (W)

Normalized Pulse Width

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Co-Design: Volume / Form Factor

Linear SM and MMIC PA in test setup

GaN PA + hybrid switcher in measurement setup

PA from Run #1 + Integrated DSM

PA from Run #1 + Cascode UHF PA for high bandwidth supply-mod.

4W PA

Cascode
# Key Performance Parameters and Milestones
## Technical Area II

<table>
<thead>
<tr>
<th>Key Performance Parameter</th>
<th>Value</th>
<th>Units</th>
<th>Today</th>
<th>6</th>
<th>12</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency of RF Power Amplification</td>
<td>≥10</td>
<td>GHz</td>
<td>2.14</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>RF Output Power</td>
<td>≥5</td>
<td>W</td>
<td>8/36</td>
<td>&gt;1W</td>
<td>&gt;5W</td>
<td>&gt;10W</td>
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<tr>
<td>Amplitude Peak-to-Average Ratio</td>
<td>≥6</td>
<td>dB</td>
<td>7</td>
<td>6</td>
<td>6dB</td>
<td>6dB</td>
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<tr>
<td>Average Composite Power-Added Efficiency</td>
<td>≥75</td>
<td>%</td>
<td>52</td>
<td>45</td>
<td>&lt;50%</td>
<td>60%</td>
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<tr>
<td>PA RF Envelope Bandwidth</td>
<td>≥500</td>
<td>MHz</td>
<td>23</td>
<td>1</td>
<td>100</td>
<td>300</td>
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</table>

Milestones met

<table>
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<tr>
<th>Simultaneous Performance Parameters</th>
<th>Value</th>
<th>Units</th>
<th>Current results</th>
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</thead>
<tbody>
<tr>
<td>Frequency of RF Power Amplification</td>
<td>≥10</td>
<td>GHz</td>
<td>10.5GHz</td>
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<tr>
<td>RF Output Power</td>
<td>≥5</td>
<td>W</td>
<td>4.5</td>
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<tr>
<td>Amplitude Peak-to-Average Ratio</td>
<td>≥6</td>
<td>dB</td>
<td>4.6</td>
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<tr>
<td>Average Composite Power-Added Efficiency</td>
<td>≥75</td>
<td>%</td>
<td>60</td>
</tr>
<tr>
<td>PA RF Envelope Bandwidth</td>
<td>≥500</td>
<td>MHz</td>
<td>5</td>
</tr>
</tbody>
</table>
6. New ideas enabled by MPC results

- High efficiency transmitter architectures for high PAR signals
  - Harmonically-injected PAs (10GHz fundamental, 20GHz output injection)
    - Simultaneous efficiency and linearity
    - Enhanced by supply modulation
  - Outphasing PAs with supply modulation
    - Performed 10-GHz nonlinear measurements internal to a Chireix combiner to understand load-pulling trajectories for next design
    - Isolated vs. non-isolated outphasing PA

- High efficiency circuits for future supply modulators
  - 500-MHz driver stage with balun feed (80% efficient)
  - Integrated UHF cascode PA with X-band PA (>80% efficient)
  - DSM4 (~60% efficient, switching at 2GHz)

- Nonlinear time-domain measurements
Harmonically-Injected PA

Baseband Signal Generation + DACs (fs)

Baseband Signal + DACs (fs)

UPAC

Mixer

2f₀ PA

O/P

f₀ PA

P_{inj}(2f₀)

P_{inj}(2f₀)

G_{2} = \frac{P_{inj}(2f₀)}{P_{inj}}

Through Port

A

B

Injection Port

10GHz

10.6GHz

Gain

PAE (%) 0 10 20 30 40 50 60 70

P_{out}(2f₀) (dBm) 0 5 10 15 20 25 30

P_{in}(2f₀) (dBm) 6 8 10 12 14 16 18 20 22

η_{total} HI-PA

η_{D} no inj

η_{total} (%) 0 10 20 30 40 50 60 70

P_{in} (dBm) 12 16 20 24 28

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Hybrid outphasing PA measurements

Single-Stage PA Performance

- Single-Stage Class-B PA
- 69% Peak PAE with 2.7 W of output power
- > 60% PAE for more than 1 GHz of bandwidth

Measurement setup with SWAP LSNA measuring PA parameters and reflection coefficients at each DUT port
- Measured load-pull contours are used to design the combiner and therefore the load modulation
Both non-isolated (a) and isolated (b) combiners utilized in hybrid outphasing.

Couplers are included in the combiner in order to measure ‘internal’ PA parameters and performance.

Designed load modulation contours on previous slide.
• Measurement setup (left) includes couplers in the combiner to measure internal PA performance and actual load modulation

• Measured load modulation (right) of non-isolated combiner (a) and isolated combiner (b)
• System performance measured with power meter and includes all losses in output combiner (reduced when integrated on chip, raising PAE by 10%)
• \(\text{PAE}_{\text{PA}1}\) and \(\text{PAE}_{\text{PA}2}\) show performance of internal PAs during outphasing
• PAE vs. Power back-off shown on right for easy visualization with signal PDF


“RFPA supply modulator using wide-bandwidth linear amplifier with a GaN HEMT output stage,” D. Li, M. Rodriguez, A. Zai, D. Sardin, D. Maksimovic and Z. Popovic, the 14th IEEE Workshop on Control and Modeling for Power Electronics, IEEE COMPEL 2013, June 23-26, Salt Lake City, Utah.

“Characterization of transistor drain supply terminal impedance at signal envelope frequencies,” Zoya Popovic, *IEEE MTT IMS 2013 workshop on low-frequency measurements for RF circuits*, Seattle, June 2013 (organizers: Jon Martins, Kate Remley)

“Co-design of power amplifier and dynamic power supplies for radar and communications transmitters,” Zoya Popovic, *IEEE MTT IMS2013 RFIC workshop on supply-modulated PAs*, Seattle, June 2013 (organizer: Donald Liu)

"High Frequency Synchronous Buck Converter using GaN-on-SiC HEMTs," M. Rodriguez, Y. Zhang, D. Maksimovic, presented at IEEE Energy Conversion Congress and Expo (ECCE), September 2013.


Z. Popovic organized workshop at RWW (January, Newport Beach) “PA design: from device model to high-performance circuit”

“Supply-modulated transmitters,” Z. Popovic et. al., invited talk at the RFIC Workshop on PAs, June, Tampa.

Z. Popovic organizing workshop at IMS (June, Florida), “Efficient amplifiers and transmitters for high peak-to-average ratio signals” (Includes several MPC performers) and similar at EuMC

Papers in preparation:
• Two papers for GOMAC Tech
• 3 papers accepted at IMS
• 3 papers submitted to EuMC
• “Supply-Modulated Transmitters for Radar with Gaussian Pulses,” Andrew Zai, Miguel Rodriguez, Zoya Popovic, submitted to IET special issue on radar

“Low-frequency measurements for supply-modulated transmitter integration,” Scott Schafer, Tibault Reveyrand, Zoya Popovic, to be submitted to the IEEE TMTT
“Wideband supply-modulated high-efficiency X-band MMICs,” David Sardin, et al., to be submitted to the IEEE TMTT or TCAS