In the circuit illustrated below, the inductor current $i_L$ flows in the direction shown, and has negligible switching ripple. The gate drivers have propagation delay times of 50 ns and are able to drive the MOSFET gate-to-source voltages with rise and fall times of 25 ns. The resulting rise and fall times of the MOSFET drain-to-source voltages are observed to be substantially faster than 25 ns. When operating in the circuit below, the total on-state charge in the MOSFET $C_{gs}$ is 4 nC, and the total off-state charge on the MOSFET $C_{gd}$ is 8 nC.

(a) The input logic signals $v_{C1}$ and $v_{C2}$ are illustrated below, for the transition in which $Q1$ is switched off and $Q2$ is switched on. Sketch the remaining three waveforms.
(b) The input logic signals $v_{C1}$ and $v_{C2}$ are illustrated below, for the transition in which $Q1$ is switched on and $Q2$ is switched off. Sketch the remaining three waveforms.

(c) As discussed in class, under certain conditions, excessive $d(v_{ds})/dt$ may cause unwanted switching of one of the MOSFETs, in which charge from $C_{gd}$ is transferred to $C_{gs}$ of sufficient magnitude to turn the MOSFET on. For which of the above transitions is this a danger? On the circuit diagram below, sketch a solution to this problem (as discussed in lecture). You should assume that the inductor current always flows in the direction indicated, and do not add more elements than necessary to solve the problem as defined here.