Experiment 3

DC-DC converter
Battery charge controller
Peak power tracker

Buck converter

Gate driver with isolation transformer

Pulse-width modulator
Micro controller

Peak power tracking and battery charge control

Sensors
Battery current and voltage
Layout issues

Example: Buck converter

Use loop analysis

Switched input current $i_1(t)$ contains large high frequency harmonics
—hence inductance of input loop is critical
inductance causes ringing, voltage spikes, switching loss, generation of B- and E-fields, radiated EMI

The second loop contains a filter inductor, and hence its current $i_2(t)$ is nearly dc
—hence additional inductance is not a significant problem in the second loop
Parasitic inductances of input loop explicitly shown:

Addition of bypass capacitor confines the pulsating current to a smaller loop:

high frequency currents are shunted through capacitor instead of input source
Even better: minimize area of the high frequency loop, thereby minimizing its inductance.
Example: gate driver

\[ i_g(t) \]
Solution: bypass capacitor and close coupling of gate and return leads

High frequency components of gate drive current are confined to a small loop
A dc component of current is still drawn output of 15V supply, and flows past the control chips. Hence, return conductor size must be sufficiently large
Averaged switch modeling
Basic approach (CCM)

Given a switching converter operating in CCM

Buck converter example

Separate the switching elements from the remainder of the converter

Define the terminal voltages and currents of the two-port switch network
Terminal waveforms of the switch network

**Relationship between average terminal waveforms:**

\[
\langle v_1(t) \rangle_{T_s} = \frac{d'(t)}{d(t)} \langle v_2(t) \rangle_{T_s}
\]

\[
\langle i_2(t) \rangle_{T_s} = \frac{d'(t)}{d(t)} \langle i_1(t) \rangle_{T_s}
\]
Averaged model of switch network

\[
\langle v_1 \rangle = \frac{d'}{d} \langle v_2 \rangle = \langle v_g \rangle
\]

\[
\langle i_2 \rangle = \frac{d'}{d} \langle i_1 \rangle = \langle i_L \rangle
\]

So

\[
\langle v_1 \rangle = \frac{d'}{d} \langle v_2 \rangle
\]

\[
\langle i_2 \rangle = \frac{d'}{d} \langle i_1 \rangle
\]
Switch Library File
Spice simulation of averaged waveforms

.subckt CCM1 1 2 3 4 5
Et 1 6 value={((1-v(5))*v(3,4)/v(5))}
Vdum 6 2 0
Gd 4 3 value={((1-v(5))*i(Vdum)/v(5))}
.ends
Basic CCM SEPIC Example
Frequency Response

Ideal SEPIC frequency response
.lib switch.lib
Vg 1 0 dc 120V
L1 1 2x 800uH
RL1 2x 2 1U
C1 2 3 100uF
L2 3 0 100uH
C2 4 0 100uF
RL 4 0 40
Vc 5 0 dc 0.4 ac 1
Rc 5 0 1M
Xswitch 2 0 4 3 5 CCM1
.ac DEC 201 10 100kHz
.PROBE
.end
AC analysis in Spice

Given a nonlinear time-invariant circuit, as on the previous slide, we can get Spice to automatically perturb, linearize, and plot small-signal ac transfer functions:

• Use DC sources to set up the correct quiescent operating conditions
• Include an AC source having amplitude 1
• Perform an AC analysis: Spice will
  • Do a DC analysis to find the quiescent operating point
  • Linearize all nonlinear elements at this point, to construct a linear model
  • Perform an AC (phasor) analysis at specified frequencies to find the magnitudes and phases of all signals
  • Construct Bode plots of selected signals. With an input amplitude of 1, the signal magnitude and phase plot is the transfer function.
AC analysis
SEPIC Example: Control-to-output transfer function
Discontinuous Conduction Mode

- Again find average values of switch network terminal voltages and currents
- Eliminate variables external to the switch network
- Results on next slides
Input (transistor) port
Averaged equivalent circuit

\[
\langle i_1(t) \rangle_{T_s} = \frac{d_1^2(t) T_s}{2L} \langle v_1(t) \rangle_{T_s}
\]

\[
\langle i_1(t) \rangle_{T_s} = \frac{\langle v_1(t) \rangle_{T_s}}{R_e(d_1)}
\]

\[
R_e(d_1) = \frac{2L}{d_1^2 T_s}
\]
Output (diode) port
Averaged equivalent circuit

\[
\langle i_2(t) \rangle_{T_s} = \frac{d_1^2(t)}{2L} \frac{T_s}{\langle v_1(t) \rangle_{T_s}^2} \langle v_2(t) \rangle_{T_s}
\]

\[
\langle i_2(t) \rangle_{T_s} \langle v_2(t) \rangle_{T_s} = \frac{\langle v_1(t) \rangle_{T_s}^2}{R_e(d_1)} = \langle p(t) \rangle_{T_s}
\]
Averaged modeling of CCM and DCM switch networks
Spice model CCM-DCM1
Combined CCM/DCM switch model

* MODEL: CCM-DCM1
* Application: two-switch PWM converters, CCM or DCM
* Limitations: ideal switches, no transformer

* Parameters:
  * L=equivalent inductance for DCM
  * fs=switching frequency

* Nodes:
  * 1: transistor positive (drain of an n-channel MOS)
  * 2: transistor negative (source of an n-channel MOS)
  * 3: diode cathode
  * 4: diode anode
  * 5: duty cycle control input

.subckt CCM-DCM1 1 2 3 4 5
+ params: L=100u fs=1E5
Et 1 2 value={((1-v(u))*v(3,4)/v(u)}
Gd 4 3 value={((1-v(u))*i(Et)/v(u)}
Ga 0 a value={MAX(i(Et),0)}
Va a b
Ra b 0 1k
Eu u 0 table {MAX(v(5), v(5)*v(5)/(v(5)*v(5)+2*L*fs*i(Et)/v(3,4)))} (0 0) (1 1)
.ends

This is one of the models inside switch.lib
It automatically switches between CCM and DCM as necessary
LTspice simulation
Exp. 3 Part 1: open loop

- Use your PV model from Exp. 1
- Replace buck converter switches with averaged switch model
- CCM-DCM1 and other Spice model library elements are linked on the course web page
- Online module and quiz on D2L