Interconnect Aware Design

Interconnect Modeling Regimes

- **Boards**
  - L >> λ
  - Classic Mixed Signal IC
  - Well Defined Ground
  - S parameters
  - Frequency Domain

- **Packages**
  - L ≈ λ
  - MMIC’s
  - RFIC-Si
  - Inductance
  - Poorly Defined Ground
  - Frequency and Time

- **Digital IC**
  - L << λ
  - Classic Microwave
  - Time Domain

- **RFIC-SOI**
  - Few Nets
  - Complexity of Interconnect

- **RFIC**
  - Large Number Nets

AWR
**"Classic" Microwave Interconnect Flow**

- Interconnect “drawn” in schematic
  - Use transmission line and discontinuity models.
    - Distributed models with phase change, dispersion,...
    - Ground plane centric models.
  - Can be awkward to draw.
  - Worried about coupling between lines.
- Rest of layout drawn as polygons.
- Post layout checking with EM tools and DRC checkers.
  - General EM simulation can be time consuming

**“Classic” Board and Package Interconnect Flow**

- Transmission lines in schematic to give delay, impedance.
  - No effort at layout - other than getting overall length.
  - Maybe some coupled line and discontinuity models

- Layout person completes layout including high speed nets.
- Final checking with EM simulation of some kind.
Interconnect Aware Design

“Classic” Analog Interconnect Design Flow

- Interconnect is a parasitic - its effects are included later in the design.
- Schematic does not show interconnect.
- Layout - interconnect is drawn as polygons.
- Through electrical “extraction” a model is created.
- The circuit is resimulated with parasitics.
- The rest of the layout is drawn.
- The circuit is checked for DRC and LVS.

Critical Interconnect Extraction Concept

- Critical analog nets are extracted quickly and accurately.
- Extracted model is placed back in simulation automatically.
- After critical nets are determined - rest of circuit is drawn and traditional DRC / LVS simulations carried out.
Models for Extraction

- **L >> \lambda**: Few Nets
  - Transmission Lines with well defined grounds
  - Phase delay
  - Loss
  - Dispersion

- **L << \lambda**: Large Number Nets
  - Lumped RLCK models
    - DC Loss (Some HF)
    - Series/Mutual Inductance
    - Mutual Capacitance

- **ACE**: Microwave
  - Inductance
  - Poorly Defined Ground
  - Frequency and Time

- **RFIC**: Transmission Lines with well defined grounds
  - Phase delay
  - Loss
  - Dispersion

- **Classic Mixed Signal IC**: Lumped RLCK models
  - DC Loss (Some HF)
  - Series/Mutual Inductance
  - Mutual Capacitance