ECEN4618: Experiment #2
Pulse-Width Modulator Design

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In the Lab #1, a simple pulse generator (astable circuit) was constructed using the integrated 555 timer. The frequency and the pulse width of the output waveform were determined by the values of the resistors and capacitors connected around the timer. In many electronic systems, there is a need for pulse generators where the pulse width, frequency, and/or amplitude can be adjusted by varying (analog or digital) input signals, without changing any component values in the circuit. Laboratory pulse generator is an example of such application, where all output signal characteristics (frequency, pulse width, and amplitude) are user-adjustable.

In this lab assignment you are going to design a periodic pulse generator where the pulse width of the output waveform is adjustable by an analog input voltage or by an 8-bit digital input. The pulse width t_H relative to the period T_s is called the duty ratio D of the output waveform. The process where the duty ratio of a pulsating signal is controlled by another input signal is called pulse-width modulation (PWM). Pulse-width modulators can be found in some types of communication systems, in controllers for switching power supplies and amplifiers, in general-purpose laboratory pulse generators, and in many other electronic systems.

Required functions of the pulse-width modulator are described in Section 1. An approach to designing the PWM circuit is discussed in Section 2. Design specifications are given in Section 3. Your laboratory tasks are described in Section 4. The prelab assignment is in Section 5.

1 Pulse-Width Modulator

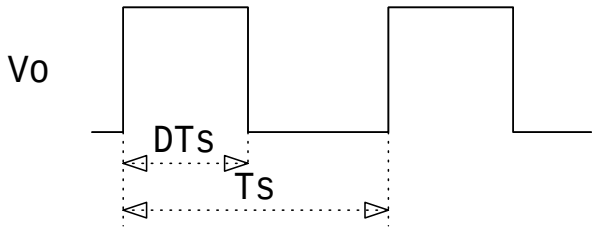
In the pulse-width modulator to be designed, the output pulse width t_H relative to the period T_s is determined by either an analog input voltage v_m, or by an 8-bit digital input

$$A = \{A_1,\, A_2,\, A_3,\, A_4,\, A_5,\, A_6,\, A_7,\, A_8\}\,, \tag{1}$$

$A_k = \{0, 1\}$.

The pulse width t_H relative to the period T_s is called the duty ratio D of the output waveform. With the analog PWM input v_m, the output duty ratio D is proportional to the to the input voltage v_m,

$$D = \frac{t_H}{T_s} = \frac{v_m}{V_M}\,, \tag{2}$$



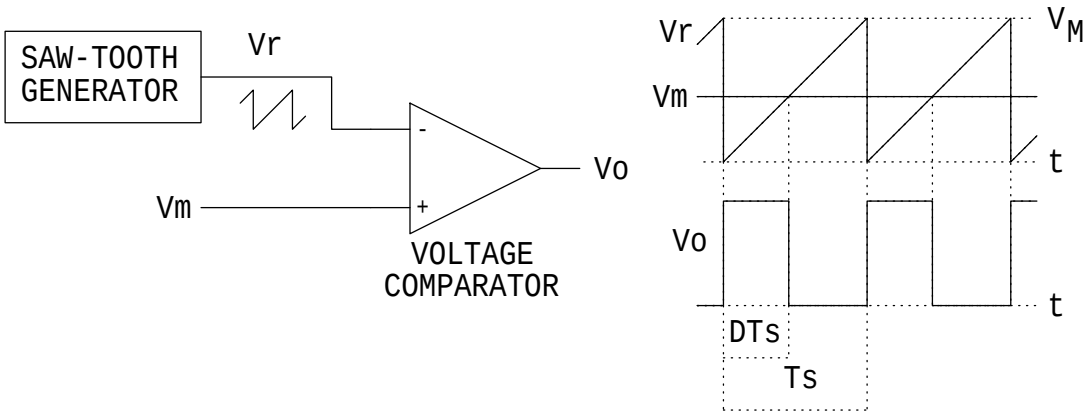


Figure 1: Pulse width modulation using a saw-tooth generator and a voltage comparator.

where V_M is a constant. The output duty ratio goes from $D = 0$ for $v_m \leq 0$, to $D = 1$ for $v_m \geq V_M$.

With the digital PWM input A, the duty ratio D is determined by the fractional binary value of A,

$$D = \frac{t_H}{T_s} = \frac{1}{256} \sum_{k=1}^{8} A_k 2^{(8-k)} \tag{3}$$

The output duty ratio should go from $D = 0$ for $A = 0$ (all 0's), to $D = 255/256$ for $A = 255$ (all 1's).

2 Designing a pulse-width modulator circuit

Given a required function of a circuit, we first consider how the function can be implemented in hardware using some known simpler building blocks. In the case of the pulse-width modulator, the required output can be obtained by comparing the analog input v_m with a periodic saw-tooth waveform $v_r(t)$, as shown in Fig. 1. If the amplitude of the saw-tooth waveform is equal to V_M, it is clear that $D = v_m/V_M$. The voltage comparator in Fig. 1 can be implemented using one of general-purpose comparator integrated circuits.

Next, it is necessary to construct the periodic saw-tooth waveform with the given period T_s and the given amplitude V_M. A conceptual solution is shown in Fig. 2. Suppose that $v_r(0) = 0$ and that the switch Q is off. The constant current source I charges the capacitor C, so that the voltage across the capacitor is given by

$$v_r(t) = \frac{I}{C} t\,, \quad t \geq 0\,, \tag{4}$$

which gives the desired linearly increasing waveshape. To get the periodic saw-tooth, the capacitor voltage must be periodically reset to zero. This function can be accomplished by turning the switch Q on and off every T_s seconds. The interval when the switch is on should be very short. In practice, it should be long enough to ensure that C is fully discharged, but much shorter than the period T_s of the saw-tooth waveform.

A variety of practical circuits can be constructed to follow the conceptual solution of Fig. 2. We will use an op-amp based circuit to achieve the near-constant current charging of the capacitor

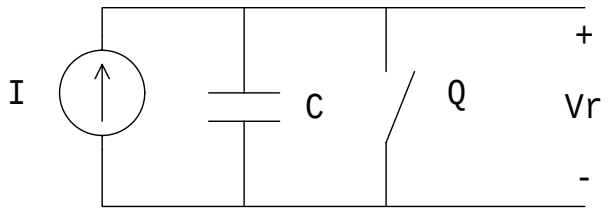


Figure 2: A conceptual saw-tooth generator.

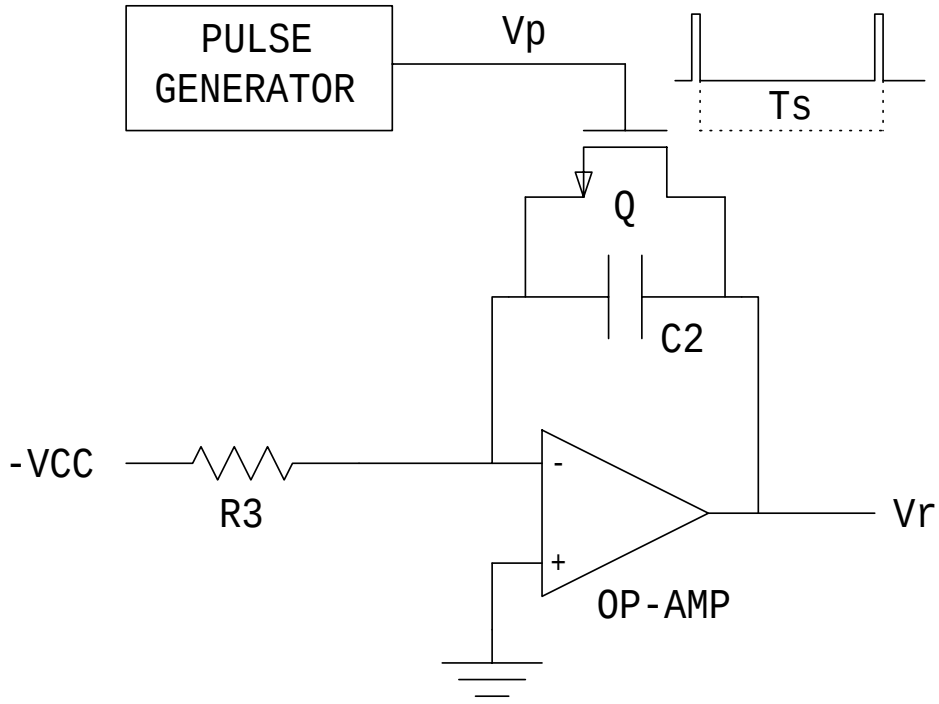


Figure 3: A saw-tooth generator using a pulse generator and an op-amp integrator with reset.

C, and an n-channel MOS transistor to serve as the reset switch Q. The circuit is shown in Fig. 3. When the MOS transistor is off, the capacitor is charged by the current

$$I \approx \frac{V_{CC}}{R_3} \tag{5}$$

The current is not exactly equal to V_{CC}/R_3 because the op-amp gain and bandwidth are finite and the $(-)$ input of the op-amp is not exactly at the zero potential (virtual ground). When the MOS transistor is turned on with a short gate pulse v_p, the capacitor is quickly discharged toward zero.

It remains to construct a pulse generator to produce very short pulses $v_p(t)$, with the period equal to T_s. Again, this function can be accomplished using a variety of techniques. For example, we can apply the 555 astable circuit, which was built and tested in the Lab #1. The same design

can be used here, except that the output should be inverted to obtain short pulses required to reset the op-amp integrator.

The building blocks: the 555 pulse generator with the inverter, the saw-tooth generator, and the voltage comparator can now be put together to construct the pulse-width modulator with analog input v_m. The digital input can be added easily using an integrated D/A converter. The D/A output replaces the analog input v_m.

A complete pulse-width modulator circuit with analog input v_m, or digital input A, is shown in Fig. 4. The active components have been selected: 555 timer for the pulse generator; a CD4093 CMOS NAND gate is used as the inverter; the op-amps are LF353 (LF353 integrated circuit has two op amps); the voltage comparator is LM311; the D/A converter is DAC0808. Discrete component values have not been assigned.

DAC0808 is an 8-bit D/A converter. With the $V_{CC} = +5$V, the inputs $A_1 - A_8$ are compatible with standard CMOS or TTL logic levels. The DAC0808 output is the current I_o given by:

$$I_o = I_{ref} \left(\frac{A_1}{2} + \frac{A_2}{4} + \cdots + \frac{A_8}{256} \right) \tag{6}$$

Resistor R_6 is connected from V_{CC} to the (+) input of an internal op-amp in the DAC0808. This input is the virtual ground node, so that the reference current $I_{ref} = V_{CC}/R_6$ is obtained in the configuration shown in Fig. 4. Resistor R_7 is connected from (-) input of the internal DAC0808 op-amp to ground. For minimum offset error, $R_7 = R_6$ should be selected. The LF353 op-amp U6 serves as a current-to-voltage converter. The output voltage is given by $v_m = R_8 I_o$.

3 Design specifications

It is required to design the pulse-width modulator using the circuit of Fig. 4, such that:

1. $v_p(t)$ is a pulsating voltage waveform with frequency $f_s = 1/T_s = 50$kHz, $\pm 2\%$, and pulse width shorter than 1μs;

2. when the analog input is selected, $v_o(t)$ is a pulsating voltage waveform with frequency $f_s = 50$kHz, $\pm 2\%$, and duty ratio D linearly dependent on the analog input voltage v_m, $D = v_m/4\text{V}$, $0 \leq v_m \leq 4\text{V}$;

3. when the digital input is selected, the duty ratio D of $v_o(t)$ is determined by:

$$D = \frac{1}{256} \sum_{k=1}^{8} A_k 2^{(8-k)} \, . \tag{7}$$

4. the rise (t_r) and the fall (t_f) times of v_o are shorter than 1μs.

Your prelab assignment is to select the component values, and prepare for experimental evaluation of the circuit in Fig. 4. In selecting components to meet a given set of specifications, it is always a good idea to break the task into several smaller and simpler tasks. In the pulse-width modulator example, one may note that the pulse generator, the saw-tooth generator, the voltage comparator, and the D/A converter are relatively independent, so that each part can be designed and tested separately.

The selection of components for the given set of design specifications is not unique. In addition to basic relations that should follow easily from the idealized component models and the discussion

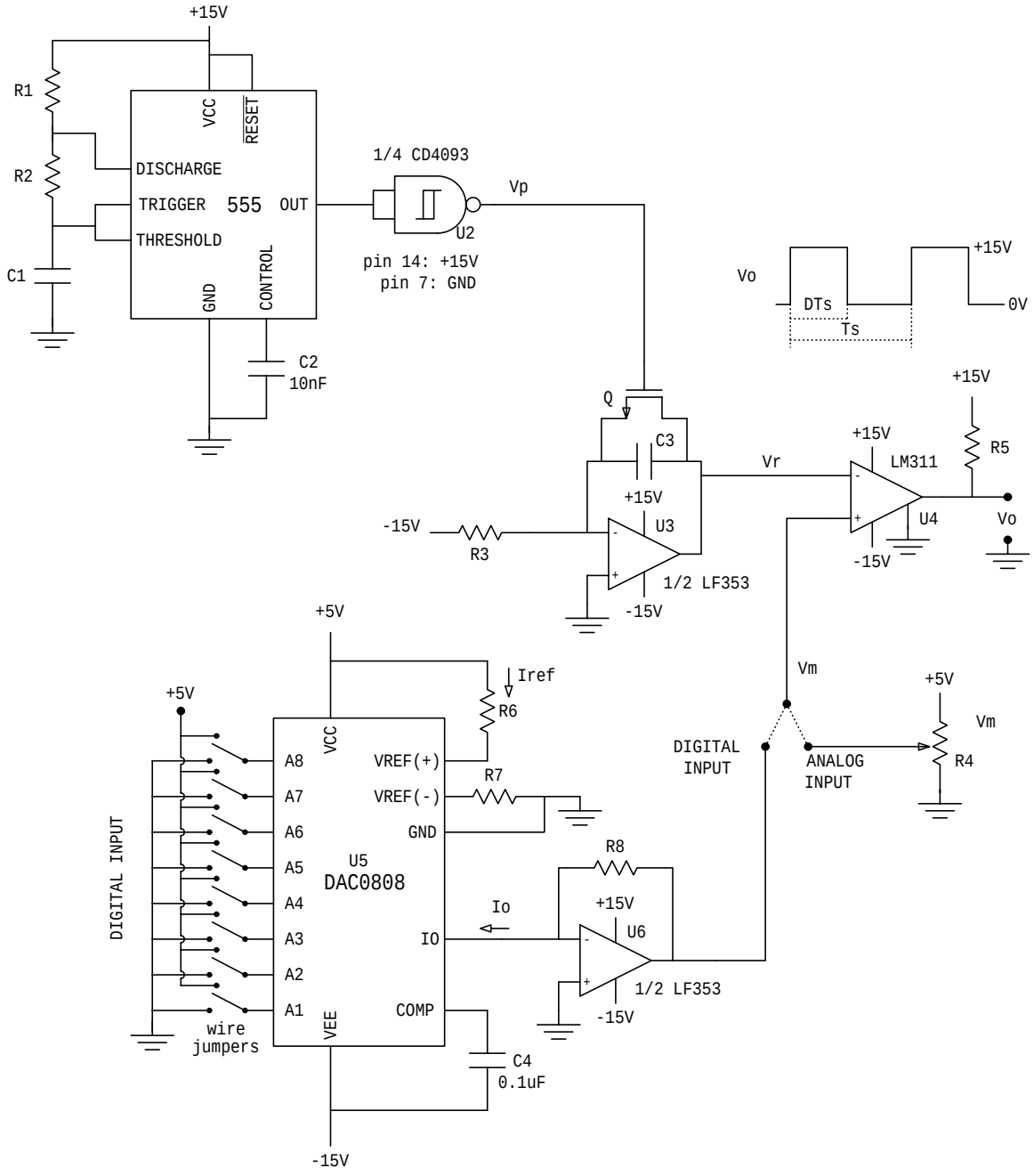


Figure 4: Complete circuit of the pulse width modulator.

above, there are many practical constraints that affect the "paper design" and/or experimental tuning later in the lab. Some of these "hidden" constraints are discussed here:

1. Discrete components are available only in standard values. A list standard resistor values with 5% tolerance can be found in the ECEN4618 Archive. Capacitor values follow the same pattern. Use only standard values in your design.

2. Values of discrete components are specified as nominal values with tolerance in %. For example, 5% is the typical tolerance for discrete resistors available in the lab.

3. The output resistance of the CMOS logic gate is not zero, and it can source or sink only up to several mA of current at the output.

4. The rise and the fall times of the 555 timer are not zero.

5. The MOS transistor is not an ideal switch. The on-resistance R_{on} of the MOS transistor used in the lab is nominally 5Ω. The MOS transistor has input and output capacitances in the order of one hundred pF. The capacitive loading may significantly affect the gate drive waveform $v_p(t)$.

6. The gain-bandwidth product of the op-amp LF353 is around 5MHz.

7. The op-amp output can source or sink up to about 10mA of current.

8. The LM311 comparator has an open-collector output. The output can sink up to about 20mA while keeping the output voltage close to zero. The output cannot source any current, so that a pull-up resistor is required.

9. The response speed of the comparator is limited. Relevant information can be found in the data sheets.

10. There is some parasitic capacitive coupling between adjacent contacts on the protoboard where the circuit is assembled. The capacitance between the contacts is in the order of pF. (This is why the protoboard is not a good medium for testing high-speed, high-frequency electronics).

11. The oscilloscope probe adds several pF between the test point and the ground.

12. Among devices in an assembled circuit there is always some parasitic coupling through the power supply lines. This coupling is mainly due to inductance of the wires that connect the power supply to the device. It can cause the circuit to oscillate or behave in unpredictable manners. To minimize the coupling, it is a common practice to place relatively large electrolitic capacitors (about 10μF or more) on the protoboard between each supply socket and ground, as well as small ceramic capacitors (about $0.1\mu F$ or more) between each supply pin and ground, as close as possible to the device.

4 Experiment

Your main task in the laboratory is to construct the pulse width modulator and to demonstrate that it meets the specifications. The next task is to make an improvement or modification of the PWM circuit, as described in Section 4.1.

The task is to be accomplished through assembling and testing the complete circuit in stages: first the 555 pulse generator, then the saw-tooth generator, the voltage comparator, and finally the D/A converter.

1. Assemble the pulse generator as designed in Task 3.2 of the Lab #1. Add the inverter at the output and verify that the pulse generator meets the specifications.

   Also, measure the rise time and the fall time of the pulses $v_p(t)$, and the frequency f_s of the waveform.

2. Assemble the saw-tooth generator and connect the gate of the MOS transistor to the previously tested pulse generator. Observe the pulses v_p after the pulse generator has been loaded with the gate of the MOS transistor. Comment on any changes in the waveshape of $v_p(t)$ after connecting the gate of the transistor Q. Measure again the rise time and the fall time of the pulses $v_p(t)$.

   Observe the output $v_r(t)$ and note any discrepancies between the actual output and the theoretical prediction. Correct the component values if needed. Get a closer view of the sharp falling edge of $v_r(t)$. Include a plot of the falling edge from the scope screen, and label the time needed to discharge the capacitor. Explain any unexpected features of $v_r(t)$. Measure and record the amplitude V_M of $v_r(t)$. Proceed only when $v_r(t)$ meets the requirements.

3. Add the voltage comparator, and the analog input v_m from the potentiometer R_4. Observe the output $v_o(t)$ and verify that the output duty ratio can be adjusted by turning R_4. Set the duty ratio to about 0.5 and measure the rise and the fall time of the output pulses. Correct the design (if needed) to meet the specifications.

   For $D = 0.5$, record and label one complete period of the waveforms v_p, v_r and v_o.

   Measure and plot the output duty ratio D as a function of the input voltage v_m set by turning R_4 in the range $0 \leq v_m \leq 5$V.

4. Assemble the D/A converter, and make a table of the values: input A (decimal), v_m, the ideal output duty ratio $D_i = A/256$, the measured output duty ratio D, and the error $\epsilon = D - D_i$, for the following (decimal) input values: $A = 0$, $A = 1$, $A = 2$, $A = 4$, $A = 8$, $A = 16$, $A = 32$, $A = 64$, $A = 127$, $A = 128$, $A = 252$, $A = 254$, $A = 255$. Attempt to adjust the circuit so that the error is $|\epsilon| \leq 1/256$. Comment on the measured error results.

4.1 Design Modifications

If you got the pulse-width modulator completed according to the specifications, you may try to improve or modify the design in several directions. You should attempt at least one of the following modifications, or propose and pursue your own idea. Extra-credit points will be given for for proposing and testing an original idea.

1. The pulse-width modulator of Fig. 4 requires three dc supply voltages: +15V, −15V, and +5V. It is desired to modify the circuit so that it operates from a single +15V supply. Draw the modified circuit and verify the operation experimentally.

2. Redesign the circuit to operate with all specified times 2 times shorter: $f_s = 100$kHz, v_p pulse width, rise and fall times of v_o less than or equal to 0.5μs. Is this feasible ? What changes in the circuit would you suggest to improve the operation at higher frequencies ? Summarize the results of your experiments.

3. The pulse-width modulator in Fig. 4 works well only at one frequency $f_s = 1/T_s = 50\text{kHz}$. To change the operating frequency without affecting other properties of the pulse-width modulator, one would have to change the frequency of v_p, and the time constant R_3C_3 *simultaneously*. In practice, this method of setting the operating frequency would not be very convenient because it requires two adjustments and/or precise discrete component matching.

   Modify the PWM circuit so that the frequency f_s can be set using only one adjustable resistor, while the output duty ratio remains $D = v_m/4$, regardless of the frequency settings. Draw the modified circuit, and explain how it works. Find the range of frequencies where the new PWM circuit works properly. Plot $D(v_m)$ for two frequencies at the extreme points of the usable frequency range.

5 Prelab Assignment

The prelab assignment is due in the lab on the day when you start working on the experiment.

Read the complete "Experiment 2" handout.

Design (on paper) the pulse-width modulator according to the design specifications of Section 3.

555, LM311 and LF353 are in the 8-pin dual-in-line packages. DAC0808 is in the 16-pin dual-in-line package. Links to the component data sheets can be found in the ECEN4618 Archive.

Turn in the circuit diagram of the pulse-width modulator with labeled component values and pin numbers on all integrated circuits. Justify selection of the discrete component values.

Do PSpice simulation of the part of your PWM circuit consisting of the integrator around the LM353 operational amplifier and the LM311 comparator. You can use an independent "pulse" voltage source to generate $v_p(t)$. The device models are available in the ECEN4618 archive. For $v_m = 2\text{V}$, turn in the plots of simulation results for $v_p(t)$, $v_r(t)$ and $v_o(t)$ during two periods and verify that your design (in simulation) satisfies the specifications.

Make a copy of your prelab work so that you can use it during the Lab sessions.