Design of a Simple High-Power-Factor Rectifier Based on the Flyback Converter

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Abstract

A simple discontinuous conduction mode (DCM) flyback converter, operated open loop, presents an effective resistive load to its power input. It is therefore well-suited as an inexpensive high-power-factor rectifier for office equipment.

An equivalent circuit model for the DCM flyback converter based on the "loss-free resistor" concept is presented. This simple model correctly describes the basic power-processing properties of the converter, including input port resistor emulation, output port power source characteristics, and control characteristics. Based on this model, steady-state design equations are described and are used in a design example.

Design of the slow output voltage feedback loop is also considered. A small-signal ac model is developed for both the resistive load and the dc-dc converter / voltage regulator load cases. In addition, a simple first-order approximation for the line current distortion and phase shift caused by 120Hz duty cycle variations is derived.

1. Introduction

The poor power factor of conventional peak detection rectifiers is becoming a problem even at the relatively low 100-200 watt level encountered in office equipment. In consequence, an office containing a number of personal computers, copiers, and other electronic equipment may require rewiring of its 120 volt distribution circuits. To avoid this, it is desirable to develop an inexpensive high-power-factor rectifier suitable for power supplies at the 100 or 200 watt level.

Numerous authors have attacked the problem of high-power-factor rectification, a few of which are listed in the references here [1-7]. Nearly all of these involve use of a control scheme which regulates the input line current to be proportional to the line voltage, as in Fig. 1. Most often, a boost converter is used, although any converter capable of voltage step-up can be employed. A second dc-dc converter is then used for isolation and load regulation. An alternative scheme [3] involves operation of a discontinuous conduction mode boost converter at constant duty cycle. Although this results in some waveform distortion, reasonably high power factors can nonetheless be obtained with a very simple control circuit.

A third scheme is discussed here, involving a simple discontinuous conduction mode (DCM) flyback converter operated at constant duty cycle [5]. It is shown that the input port of this converter behaves inherently as a resistor, and hence no additional control is needed to obtain near-unity-power-factor rectification. Transformer isolation and turns ratio can also be obtained. Additional load voltage regulation could then be obtained using a nonisolated dc-dc converter or via three-terminal linear regulators. A block diagram is shown in Fig. 2. Since output voltage regulation is not critical, the system could be further simplified by sensing the output voltage using a third

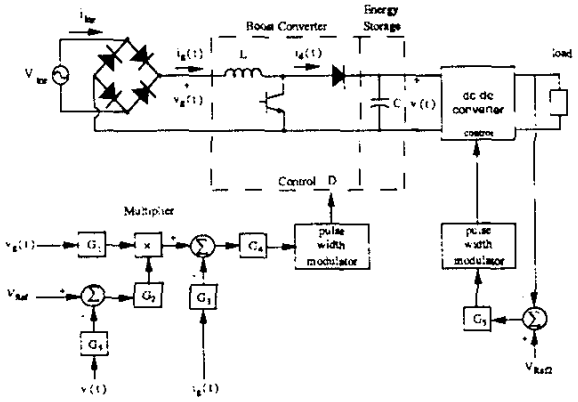

Fig. 1. A typical scheme employing a continuous conduction mode boost converter, in which the input current is actively controlled for emulation of resistive characteristics.

flyback transformer winding, connected to the primary side ground level. In this paper, the DCM flyback converter is modelled as a loss-free resistor [8], and this model is used to describe the operation of a high power factor rectifier system. A small-signal model is also derived which is suitable for design of the feedback loop necessary to stabilize the dc output voltage. A system design example is discussed and experimental results are described.

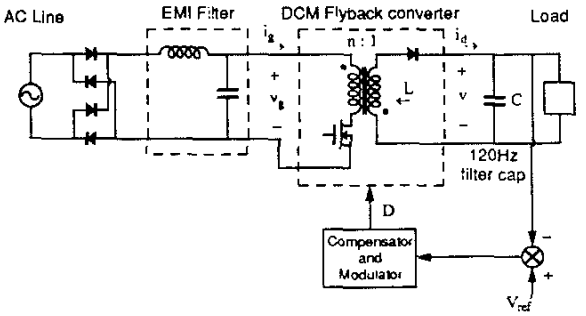

Fig. 2. Power factor correction system incorporating a flyback converter operating in discontinuous conduction mode. The system includes rectifier diodes, a high frequency emi filter, the DCM flyback converter, and a slow feedback loop to stabilize the dc output voltage.

In section 2, the "loss-free resistor" (LFR) is shown to represent the basic energy conversion properties of high power factor rectifiers in a relatively simple way. This artifice emphasizes the basic power conversion properties of ideal rectifier systems: the converter ac input port behaves as an effective resistor R_e, while the dc output port is a source of power P(t) equal to that consumed by the input port. The magnitude of the power flow is controllable by variation of R_e. Furthermore, as shown in section 3, the averaged input and output waveforms of the DCM flyback converter naturally behave in this manner, without addition of feedback. Hence, the loss-free resistor model is useful for prediction of system waveforms such as input line current, output voltage ripple, and transient response, as in section 4. These results are used in conjunction with a computer spreadsheet program in section 5 to design a flyback rectifier which operates with a given range of input voltages and load powers, and which contains transformer isolation.

As in any high-power-factor ac-dc converter, stabilization of the output voltage for changes in load current requires design of a feedback loop which controls the effective input port resistance R_e such that the dc component of the output voltage v(t) is regulated. This loop cannot attempt to remove the line frequency second harmonic (120 Hz) ripple from v(t) since this would degrade the ac line current waveform quality; hence, the crossover frequency of this loop must be much lower than 120 Hz. To design this loop, it is desired to obtain a small-signal model which correctly predicts the system waveform frequency components at the crossover frequency and below. Such a model can be obtained by averaging the system waveforms over an interval equal to the ac line frequency, and is given in section 6. In addition, a simple first-order approximation is derived which allows easy estimation of the degradation of the ac input current waveform quality by 120 Hz duty cycle variations. Generation of line current harmonics and phase shift of the fundamental component are predicted. This approximation provides a simple guideline for shaping the frequency response of the voltage feedback loop.

Operation of an experimental prototype which validates the basic modeling concepts is described in section 7. Conclusions are summarized in section 8.

2. The Ideal Rectifier

It is desired that the ideal single-phase rectifier present a resistive load to the ac system. The ac line current and voltage will then have the same waveshape and will be in phase. Unity power factor rectification is the result.

An equivalent circuit for the ac port of an ideal rectifier is therefore an effective resistance R_e, as shown in Fig. 3a. In practice, the converter may also generate switching harmonics, a nonideality which can reduce the power factor if not sufficiently filtered.

Output regulation is accomplished by variation of the effective resistance R_e, and hence the value of R_e must depend on a control signal (Fig. 3b). This allows variation of the rectifier power throughput, since the average power consumed by R_e is

$$P_{av} = \frac{V_{1,rms}^2}{R_e} \tag{1}$$

Note that changing R_e results in a time-varying system, with generation of harmonics. To avoid generation of significant amounts of harmonics and degradation of the power factor, variations in R_e and in the control input must be slow with respect to the ac line frequency.

To the extent that the converter is lossless and contains no independent internal energy storage, the instantaneous power "consumed" by R_e must appear at the converter output port.

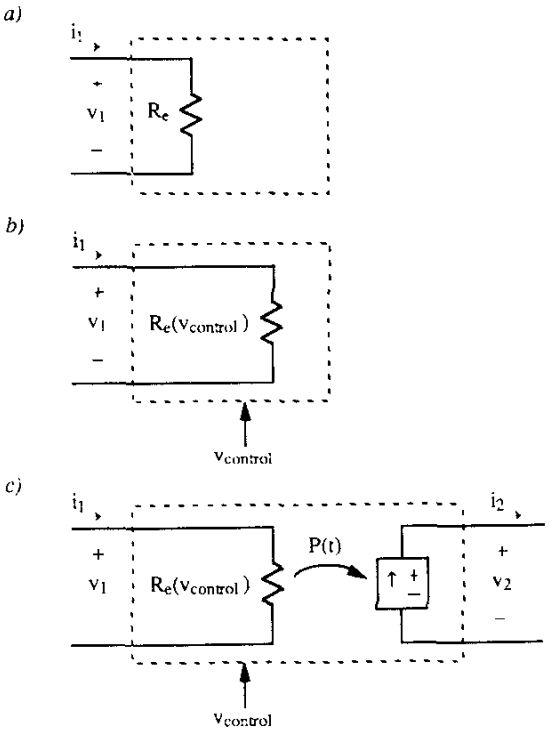

Fig. 3. Development of an equivalent circuit model for the ideal single-phase rectifier system: (a) the input port should simulate an effective resistance R_e; (b) control of the value of R_e, and hence of power flow, by a control input $v_{control}$; (c) the output port is a source of constant power P(t) equal to the input power. This two-port network is called a "Loss-Free Resistor."

Note that the instantaneous power throughput

$$\frac{v_1^2(t)}{R_e}$$

is dependent only on $v_1(t)$ and the control input, and is independent of the output port voltage and current. Hence, the output port must behave as a source of constant power, obeying the relation

$$v_2(t)\, i_2(t) = P(t) = \frac{v_1^2(t)}{R_e} \tag{2}$$

The power source symbol of Fig. 4 is used to denote such an output characteristic. Note that, unlike the basic current source or voltage source, the power source is inherently a nonlinear device. The power source must not be open- or short-circuited; this is analogous to not allowing ideal voltage sources to be short-circuited or current sources to be open-circuited.

Hence, a (nonlinear) two-port model for the ideal unity power factor single-phase rectifier is as shown in Fig. 3c. The two port model is also called a "Loss-Free Resistor" (LFR) [8] because (1) its input port obeys Ohm's Law, and (2) power entering the input port is transferred directly to the output port without loss of energy. The defining equations of the LFR are:

$$i_1(t) = \frac{v_1(t)}{R_e(v_{control})} \tag{3}$$

$$v_2(t)\, i_2(t) = P(t) \tag{4}$$

$$P(t) = \frac{v_1^2(t)}{R_e(v_{control})} \tag{5}$$

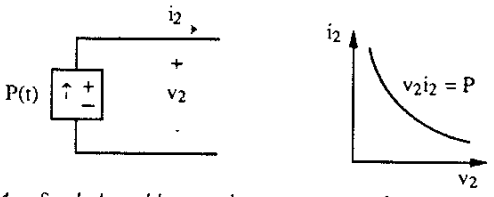

Fig. 4. Symbol used here to denote a source of constant power P(t), whose terminal voltage and current satisfy Eq. (4).

3. A Simple DCM Flyback Converter Which Obeys the LFR Equations

The buck-boost and flyback converters, when operated in discontinuous conduction mode, inherently behave as loss-free resistors. It is shown here that the low-frequency components of the terminal waveforms for these converters, operated open-loop, obey Eqs. (3)-(5).

A high power factor rectifier system employing a flyback converter operating in discontinuous conduction mode (with additional output voltage feedback) is diagrammed in Fig. 2, and typical waveforms are given in Fig. 5. Let us average the converter input and output waveforms to determine their low-frequency components [9].

The peak magnetizing current, referred to the secondary, is

$$i_{pk} = \frac{v_g(t)\, D\, T_s}{n\, L} \tag{6}$$

where L is the flyback transformer/inductor magnetizing inductance, referred to the secondary,
D is the transistor duty cycle, and
T_s is the switching period.

The converter average input current is

$$\langle i_g \rangle = \frac{1}{T_s}\int_0^{T_s} i_g(t)\, dt = \frac{D\, i_{pk}}{2\, n} \tag{7}$$

Substitution of Eq. (6) into Eq. (7) yields

$$\langle i_g \rangle = \frac{v_g(t)}{R_e} \tag{8}$$

where $R_e = 2\, n^2\, L / D^2\, T_s$ (9)

Hence, the average, or low frequency component, of the converter input current obeys Ohm's Law. The effective resistance R_e is controllable by variation of the switch duty cycle D.

The average output current is

$$\langle i_d \rangle = \frac{1}{T_s}\int_0^{T_s} i_d(t)\, dt = \frac{D_2\, i_{pk}}{2} \tag{10}$$

where $D_2\, T_s$ is the length of the output diode conduction interval. The quantity D_2 can be found by solving for the time $(D+D_2)T_s$ at which the magnetizing current reaches zero; the result is

$$D_2 = D\,\frac{v_g}{n\, v} \tag{11}$$

Substitution of Eqs. (6), (9), and (11) into Eq. (10) and rearrangement of terms yields

$$\langle i_d \rangle v = \frac{v_g^2}{R_e} \tag{12}$$

Hence, the converter output port behaves as a source of constant power

$$P = \frac{v_g^2}{R_e} \tag{13}$$

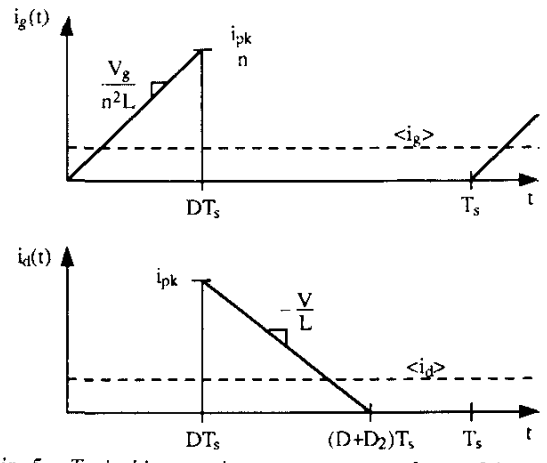

Fig. 5. Typical input and output current waveforms of the discontinuous conduction mode flyback converter cell.

equal to the power consumed by the converter input port. The loss-free resistor model of Fig. 3c applies, and an equivalent circuit for this system is given by Fig.6

Typical system waveforms are shown in Fig. 7. In a well-designed system, the EMI filter attenuates the switching harmonics of $i_g(t)$, but does not affect the low frequency components of $v_g(t)$ or $i_g(t)$. The converter input voltage is therefore a rectified sinusoid,

$$v_g(t) = V_{pk}\,|\sin \omega t| \tag{14}$$

and, by use of Eq. (9), the low frequency component of the converter input current is

$$\langle i_g(t) \rangle = \frac{V_{pk}}{R_e}\,|\sin \omega t| \tag{15}$$

Here, the input voltage $v_g(t)$ is assumed to be zero at t=0. Hence, the averaged model predicts that the instantaneous input power is

$$P(t) = v_g(t)\,\langle i_g(t) \rangle = \frac{V_{pk}^2}{R_e}\sin^2 \omega t = \frac{V_{pk}^2}{2\, R_e}(1 - \cos 2\omega t) \tag{16}$$

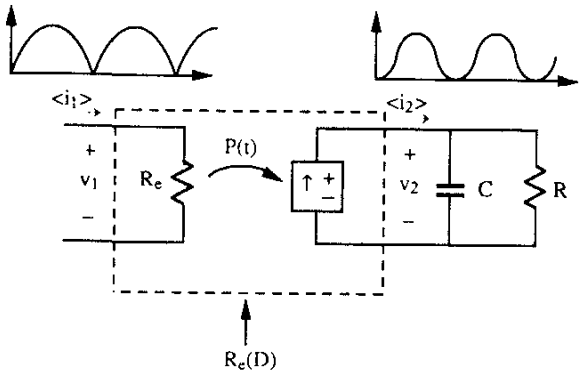

Fig. 6. Rectifier system averaged equivalent circuit. The flyback converter is modeled as a loss-free resistor.

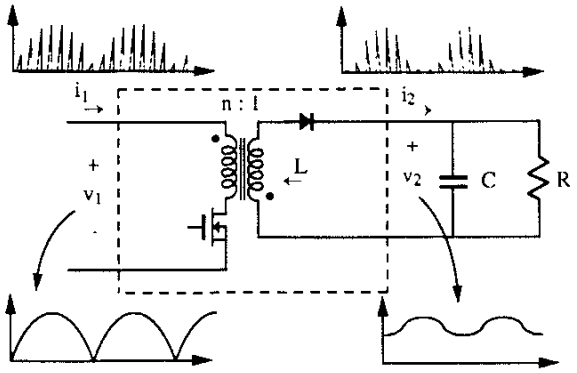

Fig. 7. Typical system waveforms.

The dc component of this is

$$P_{av} = \frac{V_{pk}^2}{2\,R_e} = \frac{V_{rms}^2}{R_e} \tag{17}$$

where V_{rms} is the rms value of the ac line voltage.

4. Solution of the System Waveforms

The equilibrium dc output voltage relations and output voltage ripple are described here for the general ideal rectifier which operates as a loss-free resistor, as well as for the specific case of the DCM flyback converter.

Power balance: ideal single-phase rectifier

The average power which flows into the input port of a converter which is controlled to behave as a loss-free resistor is given by

$$\langle P \rangle = \frac{V_{1,rms}^2}{R_e} \tag{18}$$

where $V_{1,rms}$ is the rms value of the ac input voltage. This power is transmitted to the load. In the case of a resistive load R, the output power is

$$\langle P \rangle = \frac{V_{2,rms}^2}{R} \tag{19}$$

where $V_{2,rms}$ is the rms value of the output voltage waveform. Hence,

$$\frac{V_{2,rms}}{V_{1,rms}} = \sqrt{\frac{R}{R_e}} \tag{20}$$

Similar arguments can be used to show that

$$\frac{I_{1,rms}}{I_{L,rms}} = \sqrt{\frac{R}{R_e}} \tag{21}$$

where $I_{1,rms}$ and $I_{L,rms}$ are the rms values of the input and resistive load currents, respectively.

Power balance: DCM flyback converter/rectifier

For the case of the flyback converter, Eq. (20) can be simplified by substitution of Eq. (9) to yield

$$V_{2,rms} = \frac{V_{1,rms}}{n}\,\frac{D}{\sqrt{K}} \tag{22}$$

where $K = 2L/RT_s$. With a sufficiently large output filter capacitor, $V_{2,rms}$ is essentially equal to the dc component of the output voltage, and Eq. (22) is the solution for the dc output. It is interesting that Eq. (22) is of the same form as the familiar solution for the dc-dc flyback converter, such as in [9], except that ac rms quantities are substituted for the dc voltages. Hence, the dc output voltage of the DCM flyback rectifier is a linear function of converter duty cycle and rms ac input voltage.

Output voltage ripple

With a sufficiently large output filter capacitor C, the peak output voltage ripple Δv is small compared to the dc component of output voltage V. The power source P(t) then operates at nearly constant voltage, and the output current is given by

$$i_2(t) \cong \frac{P(t)}{V} = \frac{V_{1,rms}^2}{R_e\,V}\,(1 - \cos 2\omega t) \tag{23}$$

With small voltage ripple $\Delta v \ll V$, the ac component of $i_2(t)$ flows essentially through the output filter capacitor C while the dc component flows into the load. Hence, the output filter capacitor current is given by

$$C\,\frac{dv_2(t)}{dt} = -\frac{V_{1,rms}^2}{R_e\,V}\cos 2\omega t \tag{24}$$

The magnitude of the peak voltage ripple Δv can be found by integration of this expression and substitution of Eq. (20). The result is

$$\Delta v \cong \frac{V}{2\omega RC} \tag{25}$$

This approximation is valid provided that $2\omega RC \gg 1$. It states that the output RC natural frequency should be chosen sufficiently slower than the ac line second harmonic frequency 2ω. In the case where output capacitor equivalent series resistance is significant, Eq. (25) becomes

$$\frac{\Delta v}{V} \cong \sqrt{\left(\frac{esr}{R}\right)^2 + \left(\frac{1}{2\omega RC}\right)^2} \tag{26}$$

An exact solution of the steady-state ripple waveforms, as well as the open-loop transient response, is also possible. The converter output node equation is

$$C\,\frac{dv_2(t)}{dt} = i_2(t) - \frac{v_2(t)}{R} \tag{27}$$

Substitute $i_2(t) = P(t) / v_2(t)$, and multiply by $v_2(t)$:

$$C\,v_2(t)\,\frac{dv_2(t)}{dt} = P(t) - \frac{v_2^2(t)}{R} \tag{28}$$

This equation states that the power flowing into the output filter capacitor C is equal to the difference between the converter power throughput P(t) and the load power $v_2^2(t) / R$. Although this equation is nonlinear in $v_2(t)$, it can nonetheless be solved exactly using energy arguments. Let $E_C(t)$ be the energy stored in the output capacitor:

$$E_C(t) = \frac{1}{2}\,C\,v_2^2(t) \tag{29}$$

Then the power flowing through the output capacitor is:

$$\frac{dE_C(t)}{dt} = C\,v_2(t)\,\frac{dv_2(t)}{dt} \tag{30}$$

with

$$v_2(t) = \sqrt{\frac{2\,E_C(t)}{C}} \tag{31}$$

Elimination of $v_2(t)$ from Eq. (28) yields

$$\frac{dE_C(t)}{dt} = P(t) - \frac{2E_C(t)}{RC} \tag{32}$$

which is a linear first-order differential equation. The solution is

$$E_C(t) = E_C(0)\,e^{-2t/RC} + \int_0^t e^{2(\tau - t)/RC}\,P(\tau)\,d\tau \tag{33}$$

Substitution of Eqs (16) and (31) yields the solution for the output voltage,

$$v_2(t) = \sqrt{v_2^2(0)\,e^{-2t/RC} + \frac{R}{R_e}\,V_{1,rms}^2\left\{(1 - e^{-2t/RC}) + \frac{1}{1+(\omega RC)^2}\left[e^{-2t/RC} - \cos 2\omega t - \omega RC \sin 2\omega t\right]\right\}} \tag{34}$$

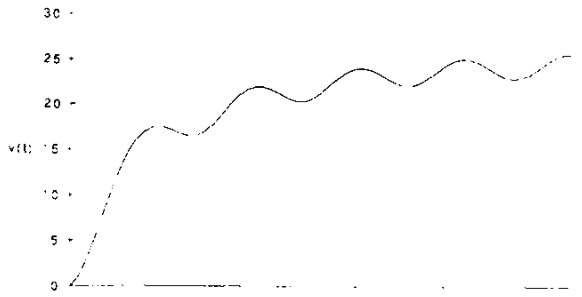

Fig. 8. A typical output voltage turn-on transient waveform, as given by Eq. (33).

A typical turn-on transient voltage waveform is plotted in Fig. 8 for the values

$$v_2(0) = 0$$
$$\omega RC = 10$$
$$V_{1,rms}\sqrt{\frac{R}{R_e}} = 25 \text{ volts}$$

It can be seen that the output voltage waveform contains transient, rectification ripple, and steady-state dc components.

The exact steady-state solution can also be found. For large t, Eq. (34) becomes

$$v_2(t) \rightarrow \sqrt{\frac{R}{R_e}}\, V_{1,rms}\sqrt{1 - \frac{\cos 2\omega t + \omega RC \sin 2\omega t}{1+(\omega RC)^2}} \qquad (35)$$

The peak ripple can be shown to be

$$\Delta v = \sqrt{\frac{R}{R_e}}\,\frac{V_{1,rms}}{2}\left\{\sqrt{1+\frac{1}{\sqrt{1+(\omega RC)^2}}} - \sqrt{1-\frac{1}{\sqrt{1+(\omega RC)^2}}}\right\} \qquad (36)$$

This expression is compared with the approximate relation, Eq. (25), in Fig. 9. It can be seen that the two equations indeed give the same results for $\omega RC >> 1$.

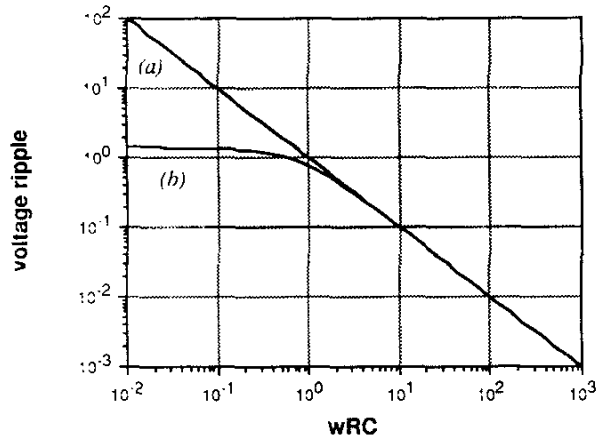

Fig. 9. Peak output voltage rectification ripple Δv/V: (a) approximate relation, Eq. (25); (b) exact relation, Eq. (36).

5. Design Example

Given the desired steady state output voltage V, the peak input voltage range $V_{pk,max} \geq V_{pk} \geq V_{pk,min}$, the range of average output power $P_{max} \geq \langle P(t)\rangle \geq P_{min}$, and the switching period T_s, the designer must determine the flyback transformer turns ratio n, the flyback inductance L (referred to the secondary), and the transistor and diode stresses. Expressions for these quantities are given here, and a comparison is made of the designs using various turns ratios for a sample set of specifications.

To maintain a sinusoidal input current, the converter must operate in the discontinuous conduction mode over the entire cycle. Referring to Fig. 5, the converter operates in discontinuous conduction mode provided that the flyback inductor current reaches zero before the end of the switching period. This can be expressed as

$$D_2 < 1 \quad D \qquad (37)$$

where
$$D_2(t) = D\,\frac{v_g(t)}{n\,v(t)} \qquad (38)$$

Hence, in a given switching period, the converter operates in discontinuous conduction mode provided that

$$D\left(1 + \frac{v_g(t)}{n\,v(t)}\right) < 1 \qquad (39)$$

The transistor duty cycle D, output voltage v, and turns ratio n are all presumed to be constant. However, the input voltage $v_g(t)$ is a rectified sine wave which varies between 0 and V_{pk}. Hence, the converter will always operate in discontinuous conduction mode provided that

$$D < \frac{1}{\left(1 + \frac{V_{pk}}{n\,V}\right)} \qquad (40)$$

From the converter steady state solution, Eq. (22), one can determine the duty cycle which produces the desired output voltage V for a given peak input voltage V_{pk}:

$$D = \frac{n\,V}{V_{pk}}\sqrt{2K} \qquad (41)$$

with
$$K = 2L/RT_s \qquad (42)$$

Elimination of D from Eqs. (40) and (41), and solution for K and L yields

$$K < K_{crit} = \frac{1}{2\left(1 + \frac{n\,V}{V_{pk}}\right)^2} \qquad (43)$$

$$L < L_{crit} = \frac{R\,T_s}{4\left(1 + \frac{n\,V}{V_{pk}}\right)^2} \qquad (44)$$

The worst case occurs with minimum load resistance R (maximum power throughput) and minimum peak line voltage V_{pk}. Hence, the secondary flyback inductance L should be chosen to be

$$L < L_{crit,\,min} = \frac{R_{min}\,T_s}{4\left(1 + \frac{n\,V}{V_{pk,min}}\right)^2} \qquad (45)$$

The designer should choose a value of L which satisfies this equation.

The rms transistor current can be shown to be

$$I_{T,rms} \equiv \frac{V_{pk}}{n^2 L} DT_s\sqrt{\frac{D}{6}} \qquad (46)$$

which is greatest at minimum ac line voltage and maximum load power. The transistor blocking voltage is

$$nV + V_{pk,max} \qquad (47)$$

The rms diode current can be shown to be

$$I_{D,rms} \equiv \frac{2}{3}(2K)^{0.75}\,\frac{VT_s}{L}\sqrt{\frac{I}{\pi}} \qquad (48)$$

which is maximum at maximum load current. The diode

n	L	K		Duty Cycle D				trans	diode	trans	diode	trans	diode
	ref to sec	min I	max I	max I Vp	max I	max Vp	min I Vp	bl vltg	bl vltg	max ipk	max ipk	max Irms	max Irms
1	7.50E-06	0.0521	0.2606	0.088	0.144	0.039	0.064	222	222	23.1	23.1	3.6	7.4
2	5.52E-06	0.0383	0.1915	0.150	0.247	0.067	0.11*	246	123	13.5	26.9	2.7	8.0
3	4.22E-06	0.0293	0.1467	0.197	0.324	0.088	0.145	270	90	10.3	30.8	2.4	8.5
4	3.34E-06	0.0232	0.1159	0.233	0.385	0.104	0.172	294	73	8.7	34.6	2.2	9.0
5	2.70E-06	0.0188	0.0939	0.263	0.433	0.117	0.193	318	64	7.7	38.5	2.1	9.5
6	2.24E-06	0.0155	0.0776	0.287	0.472	0.128	0.211	342	57	7.0	42.3	2.0	10.0
7	1.88E-06	0.0130	0.0652	0.306	0.505	0.137	0.226	366	52	6.6	46.1	1.9	10.4
8	1.60E-06	0.0111	0.0556	0.323	0.533	0.145	0.238	390	49	6.2	50.0	1.9	10.9
9	1.38E-06	0.0096	0.0479	0.338	0.556	0.151	0.249	414	46	6.0	53.8	1.8	11.3
10	1.20E-06	0.0084	0.0418	0.350	0.577	0.157	0.258	438	44	5.8	57.7	1.8	11.7
12	9.37E-07	0.0065	0.0325	0.371	0.611	0.166	0.273	486	40	5.4	65.4	1.7	12.4
15	6.77E-07	0.0047	0.0235	0.394	0.649	0.176	0.290	558	37	5.1	76.9	1.7	13.5
17	5.59E-07	0.0039	0.0194	0.406	0.669	0.182	0.299	606	36	5.0	84.6	1.7	14.1
20	4.33E-07	0.0030	0.0150	0.420	0.693	0.188	0.310	678	34	4.8	96.1	1.6	15.1
25	3.01E-07	0.0021	0.0104	0.438	0.721	0.196	0.323	798	32	4.6	115.3	1.6	16.5

Fig. 10. Use of computer spreadsheet to compare various 100W converter designs.

blocking voltage is

$$V + V_{pk,max}/n \tag{49}$$

The designs at various values of turns ratio n can be evaluated using the above equations. The results are shown in Fig. 10 for the specifications

rms line voltage:	85-140 V rms
output voltage:	24 V nominal
output power:	20-100 W
switching frequency:	100 kHz

The flyback inductance L was chosen to be 75% of $L_{crit,min}$ calculated from Eq. (45). The values of the parameter K were then calculated at the maximum and minimum load power points using Eq. (42), and the ideal transistor duty cycle was calculated at the maximum and minimum line voltage and load power points using Eq. (41). The transistor and diode worst case stresses were then determined using Eqs. (46)-(49), (42), and (6).

Based on these numbers, values of n close to 5 appear to give a good compromise between low primary side and low secondary side component stresses. It can be seen from Fig. 10 that this choice will yield rms transistor and primary winding currents of 2.1A, and rms diode and secondary winding currents of 9.5A. The peak transistor voltage is 318V, plus an additional amount from ringing caused by transformer leakage inductance.

6. Design of the Output Voltage Feedback Loop

Although the DCM flyback converter is capable of rectification when operated open-loop, it is nonetheless desirable to stabilize the output voltage against variations in load power, ac line voltage, and component characteristics. Hence, a voltage feedback loop is necessary. This loop cannot attempt to remove the 120Hz ripple from the output voltage, since doing so would require that D(t) and $R_e(D)$ change significantly at 120Hz. This would introduce significant distortion, phase shift, and power factor degradation into the ac line current waveform. In consequence, the crossover frequency of this loop must be significantly lower than 120Hz.

A small-signal model is described here which correctly predicts the control-to-output transfer function and output impedance of both the DCM flyback converter/rectifier and the general loss-free resistor. It neglects the complicating effects of switching harmonics and 120Hz ripple, and is valid for frequencies sufficiently less than 120Hz. Both resistive and dc-dc converter/regulator loads are treated. In addition, a simple estimate of the effects of 120Hz duty cycle variations on the ac line current waveform quality is made; this estimate can be used to determine how large the feedback gain at 120Hz can be made without seriously degrading the power factor.

Small signal ac model

The steps in the derivation of a small-signal ac model, suitable for design of the output voltage feedback loop, are summarized in Fig. 11. Figure 11a is the result from sections 2 and 3: the converter switching harmonics are removed, but waveform frequency components slower than the switching frequency are correctly modeled, including the 120 Hz and dc components of output voltage. It is difficult to use this model in design of the feedback loop because it is highly nonlinear and time-varying.

Since the feedback loop crossover frequency must be much slower than 120 Hz, let us not attempt to model the 120 Hz output ripple. This ripple can be removed from the output portion of the converter model by averaging over one period of the 120 Hz waveform; the result is that the power source P(t) is replaced by its sub-120 Hz frequency components,

$$\langle P(t) \rangle = \frac{V_{1,rms}^2}{R_e(D)} \tag{50}$$

Upon averaging in this manner, the output node equation (Eq. (28)) becomes

$$C\, v_2(t) \frac{dv_2(t)}{dt} = \langle P(t) \rangle - P_{load}(t) \tag{51}$$

The final step is perturbation of the waveforms about a quiescent operating point and linearization of the result. One then obtains the dc model of Fig. 11b (drawn for the case of a resistive load) and the small-signal ac model of Fig. 11c. The coefficients used in the model are summarized in Tables 1 and 2. Figure 11b is useful for determining the quiescent operating point; no information regarding dc conditions can be inferred from Fig. 11c. Figure 11c is useful for determining the various ac transfer functions. The ac resistance r_2 is derived from the slope of the $\langle P(t) \rangle$ power source output characteristic, evaluated at the quiescent operating point. The other coefficients, j_2 and g_2, are also derived from the slopes of the $\langle P(t) \rangle$ characteristic, taken with respect to D(t) and $V_{1,rms}$ and evaluated at the quiescent operating point.

The control-to-output transfer function is

$$\frac{\hat{v}_2(s)}{\hat{d}(s)} = j_2\, R \| r_2 \, \frac{1}{1 + sC\, R \| r_2} \tag{52}$$

where $\hat{d}$ is a small variation in the duty cycle, and $\hat{v}_2$ is the resulting output voltage variation. The line-to-output transfer function is

$$\frac{\hat{v}_2(s)}{\hat{v}_{1,rms}(s)} = g_2\, R \| r_2 \, \frac{1}{1 + sC\, R \| r_2} \tag{53}$$

Here, the ac line voltage is assumed to be of the form

$$v_1(t) = \sqrt{2}\, (V_{1,rms} + \hat{v}_{1,rms}(t)) \sin(\omega t) \tag{54}$$

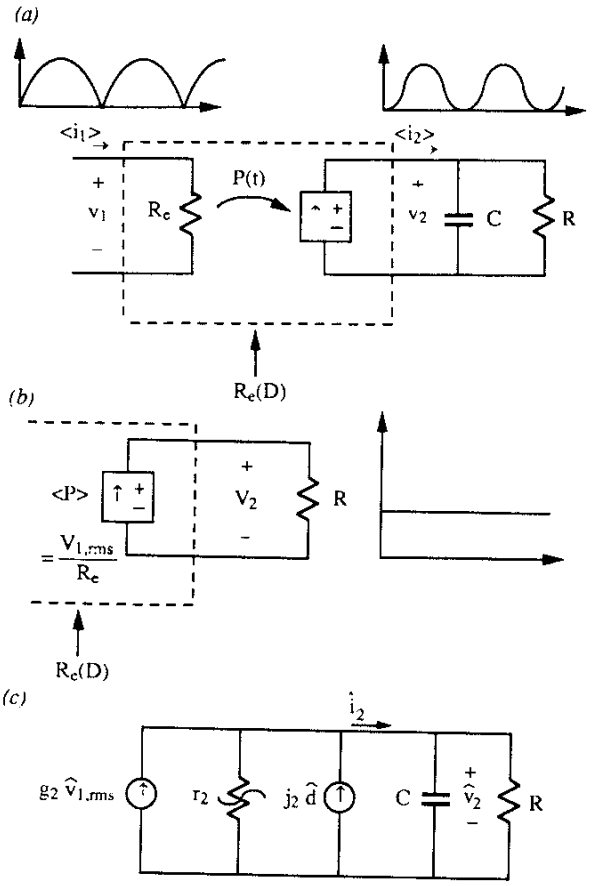

Fig. 11. Steps in the derivation of converter dc and small-signal ac models, suitable for voltage feedback loop design: (a) Basic loss-free resistor model, with switching harmonics removed, but 120Hz and dc components retained; (b) Dc model, with 120Hz components removed; (c) Small-signal ac model.

and hence $\hat{v}_{1,rms}(t)$ represents a slow disturbance in the rms amplitude of the ac line voltage.

Thus, the small-signal transfer functions of the DCM flyback rectifier contain a single pole, ascribable to the output filter capacitor operating in conjunction with the load resistance and r_2, the effective output resistance of the <P(t)> power source. Although this model is based on the LFR concept, its form is similar to that of the dc-dc DCM buck-boost converter ac model [9,10]. The major difference is that the rms value of the ac input voltage must be used, and that the 120 Hz output voltage ripple must be removed via averaging. Nonetheless, the equivalent circuit and ac transfer functions are of the same form.

An estimate of the effects of 120 Hz variations in D(t)

How large can the 120 Hz variations in the duty cycle D(t), caused by the output voltage feedback, be before the ac line current waveform is significantly degraded? How large can we allow the loop gain to be at 120 Hz? Solution of the large-signal closed-loop waveforms in general is difficult. However, we can obtain an estimate of the line current distortion and phase shift in the open-loop case where this distortion is not too large.

Table 1. Small Signal AC Model Parameters for General LFR Rectifier Network

g_2	j_2	r_2
$\frac{2}{\sqrt{R}\sqrt{R_e}}$	$\frac{V_{1,rms}^2}{V_2 R_e^2}\frac{\partial R_e}{\partial D}$	R

with $V_2 = V_{1,rms}\sqrt{\frac{R}{R_e}}$

Table 2. Basic Relations for DCM Flyback Rectifier

R_e	$\frac{\partial R_e}{\partial D}$	V_2
$\frac{2n^2L}{D^2T_s}$	$-\frac{2}{D}R_e$	$\frac{V_{1,rms}}{n}\frac{D}{\sqrt{K}}$

Suppose that the converter operates open-loop with the duty cycle waveform

$$D(t) = D_0 + \varepsilon \sin(2\omega t + \varphi) \qquad (55)$$

Here, D_0 is the quiescent operating point (dc component), $\varepsilon \sin(2\omega t + \varphi)$ is the 120 Hz component, and φ is the phase shift of the duty cycle variation with respect to the ac line voltage. This 120 Hz component of D(t) may be estimated knowing the output voltage ripple and the magnitude and phase of the feedback connection gain at 120 Hz. The input line current is then

$$i_g(t) = \frac{v_g(t)}{R_e(D(t))} = \frac{V_{pk}T_sD^2(t)}{2n^2L}\sin(\omega t) \qquad (56)$$

This expression neglects any additional distortion caused by the input rectifier diodes and EMI filter. Substitution of Eq. (55) into Eq. (56), application of some trigonometric identities, and rearrangement of terms yields

$$i_g(t) = \frac{V_{pk}}{R_e(D_0)}\Big[\overbrace{\sin(\omega t)}^{\text{desired component}} + \overbrace{\frac{\varepsilon}{D_0}\cos(\omega t + \varphi)}^{\text{fundamental phase shift term}} - \underbrace{\frac{\varepsilon}{D_0}\cos(3\omega t + \varphi)}_{\text{third harmonic}} + \underbrace{\text{terms of order } \varepsilon^2}_{\text{small terms}}\Big] \qquad (57)$$

It can be seen that the ratio of third harmonic magnitude to fundamental magnitude is approximately (to first order in ε):

$$\varepsilon / D_0 \qquad (58)$$

Hence, a 10% peak variation in D(t) yields a third harmonic amplitude of approximately 10% of the fundamental.

In addition to generation of harmonics, it can be seen from Eq. (57) that 120 Hz duty cycle variations can introduce phase shift into the fundamental component of the line current, given by (to first order):

$$\angle i_g(t) \cong -\tan^{-1}\left(\frac{\varepsilon}{D_0}\cos(\varphi)\right) \qquad (59)$$

Typically, φ is close to 180°, and this expression reduces to

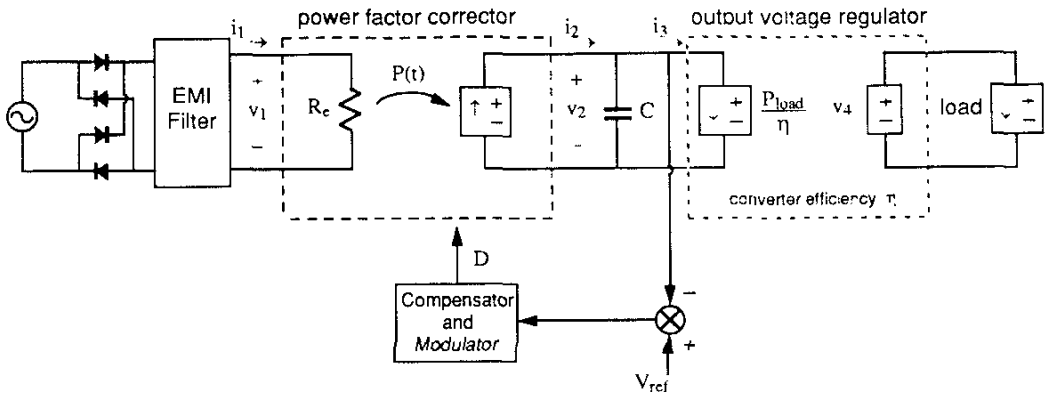

Fig. 12. Functional system diagram of flyback rectifier driving a voltage regulator as a load. The voltage regulator is constructed using a high efficiency dc-dc converter, and effectively behaves as a constant power load at low frequencies.

$\tan^{-1}(\varepsilon/D_0)$. Hence, a 10% peak 120Hz variation in D(t) yields a line current phase shift of approximately $\tan^{-1}(0.1)$, or 5.7°.

Example

Consider a design in which the converter operates at a quiescent (dc component) duty cycle of 0.25 and a quiescent output voltage V of 25 volts. The output $1/2\pi RC$ natural frequency is chosen to be 6Hz, and hence the output 120Hz peak voltage ripple is estimated using Eq. (25) to be

$$\Delta v \cong (25 \text{ volts})(6 \text{ Hz})/(120 \text{ Hz}) = 1.25 \text{ volts} \quad (60)$$

The 120 Hz component of the converter output current $i_d(t)$ lags the input line voltage by 90°, and the output capacitor voltage lags $i_d(t)$ by another 90°, so the phase is shifted by 180°. The feedback connection for this example consists of a voltage divider, reference summing node, proportional-plus-integral controller, and pulse-width modulator, whose composite output-voltage-to-duty-cycle gain at 120Hz is 0.05 volt^{-1} with negligible phase shift. Hence, the magnitude of the 120Hz duty cycle variation is estimated to be

$$\varepsilon = (1.25 \text{ volt})(0.05 \text{ volt}^{-1}) = 0.0625 \quad (61)$$

with a phase shift of

$$\varphi \cong 180° \quad (62)$$

Equation (58) predicts that the line current third harmonic relative amplitude will be $\varepsilon/D_0 = (0.0625)/(0.25)$, or 25% of the fundamental. In addition, the fundamental component is shifted in phase by $\tan^{-1}(\varepsilon/D_0) = 14°$. Although these are first order estimates which may have substantial error, they are nonetheless indicative of a significant degradation of the line current waveform.

To improve the waveform quality, the magnitude of the 120Hz duty cycle variation must be reduced. One relatively easy way to do this is to introduce additional high frequency poles into the compensator which reduce the gain at 120Hz without significantly affecting the loop gain at its crossover frequency. Alternatively, one could (1) decrease the overall compensator gain, which also decreases the regulator bandwidth, or (2) increase the output capacitance, which decreases Δv and hence ε, but increases the filter capacitor size.

Thus, Eqs. (58) and (59) provide simple estimates of the effect of 120 Hz duty cycle variations on the input line current waveform quality.

Driving a dc-dc converter / voltage regulator as a load

The model of Fig. 11c is changed somewhat when a high efficiency dc-dc converter is connected for regulation of the load voltage. It is well-known [11] that the power input of this second converter behaves nearly as a sink of constant power, equal to P_{load}/η, with a negative incremental resistance. A functional system diagram is shown in Fig. 12. The voltage regulation feedback loop of this second converter is typically several orders of magnitude faster than that of the power factor corrector slow voltage feedback loop, and hence it is a good approximation to model the voltage regulator input in this idealized manner.

The slow feedback loop for stabilization of v_2 is now essential. Any imbalance between P, the output power of the power factor corrector, and P_{load}/η, the input power drawn by the voltage regulator converter, results in a change of stored energy in capacitor C. This may cause a problem if the load power changes quickly. For example, if the load power is decreased, than P will be greater than P_{load}/η, and the excess energy will charge capacitor C. Hence, v_2 will increase, until eventually the slow feedback loop reduces the duty cycle D and causes the powers P and P_{load}/η to balance. If the feedback loop operates slowly compared to the rate at which the capacitor charges, then very large transient peak values of v_2 may be observed.

The small-signal ac model of Fig. 11c can be modified to account for the constant-power-type load P_{load}/η. The result is shown in Fig. 13. The expressions for r_2, g_2, and j_2 are unchanged, and are given by Table 1. The quantity $-r_3$ is the negative incremental input resistance of the voltage regulator

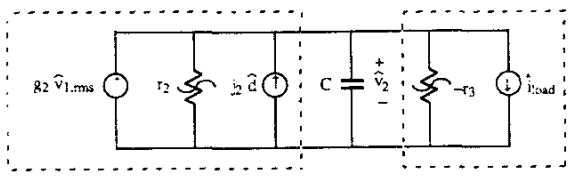

Fig. 13. Small-signal ac model of the system of Fig. 12.

converter; it is given by

$$-r_3 = \left(\frac{di_3}{dv_2}\right)^{-1} = \left(\frac{d}{dv_2}\left(\frac{P_{load}}{\eta v_2}\right)\right)^{-1} \qquad (63)$$

evaluated at the quiescent operating point. If the output converter efficiency η is independent of v_2, then $-r_3$ is equal in magnitude (but opposite in polarity) with r_2. The two resistors then cancel, and there is no net damping of the capacitor voltage v_2. For the more realistic case when η increases as v_2 increases, then the magnitude of $-r_3$ is less than v_2, and there is some small net positive damping.

Thus, an output voltage regulator can be treated using the same concepts. The output voltage regulator appears nearly as a constant power sink. Its small signal model is dominated by a negative resistor $-r_3$ which nearly cancels the power factor corrector incremental output resistance r_2.

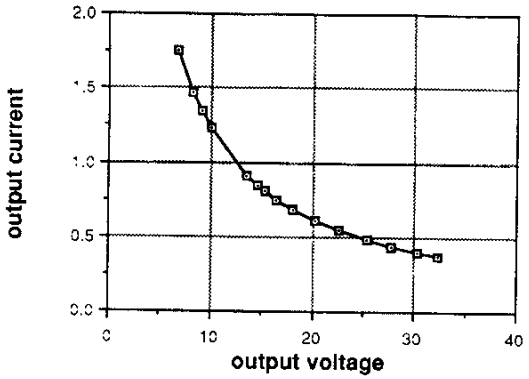

Fig. 14. Measured flyback converter/rectifier output characteristics, for operation at constant duty cycle. The output power is nearly independent of load impedance.

7. Experimental Verification

To test the validity of the basic loss-free resistor model, a 50W DCM flyback converter as in Fig. 2 was designed for operation from the 120V rms ac line. The flyback transformer turns ratio was 36:13, so that n = 2.77, and the magnetizing inductance was L = 17.3 μH referred to the secondary. The switching frequency was 50kHz, and the output capacitance was C = 3200 μF. The EMI filter was a single-section LC filter using the values 1.9 mH and 0.13 μF; these values were chosen so that an essentially resistive load was presented to the diode rectifiers at 120Hz. It was later observed that the filter Q-factor must additionally be kept reasonably low; otherwise, the ringing of the filter can substantially degrade the line current waveform quality.

First, the equilibrium output characteristics were measured. The converter was operated at a constant duty cycle of 0.12 and an ac line voltage of 120V rms. From Eq. (9), the effective ac input port resistance was therefore $R_e = 922\Omega$. The average input power should be $V_{1,rms}^2 / R_e = 15.6$W, and this power, less losses in the diode rectifiers, EMI filter, and converter, should appear at the output. The measured dc output characteristics are plotted in Fig. 14. It can be seen that the converter output port does indeed behave very nearly as a source of constant dc power. The actual measured power varied between 11.9W and 12.4W for load resistances varying from 3.9Ω to 88Ω.

The voltage conversion ratio was measured next. The load resistance was set to a constant R = 15Ω, and the duty cycle varied from 0 to 0.3. The dimensionless parameter K in this

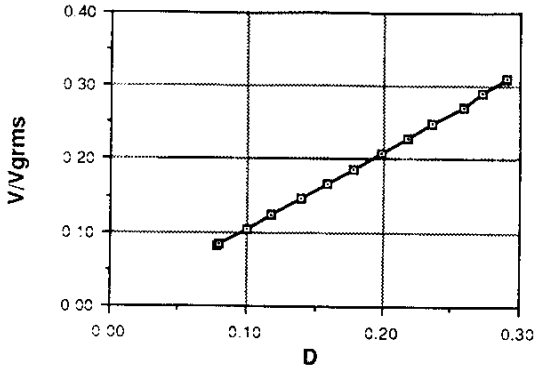

Fig. 15. Measured flyback converter/rectifier dc control characteristics, for a constant 15Ω load.

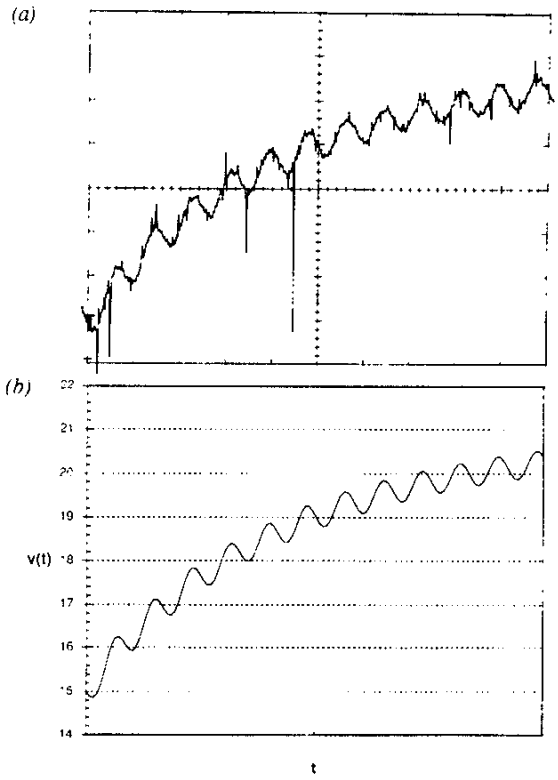

Fig. 16. Transient output voltage waveform, for a step change in load resistance from 15Ω to 30Ω. Horizontal scale: 10ms/div, vertical scale: 1V/div. (a) measured waveform, (b) waveform predicted by Eq. (34).

case is 0.1153, and the output voltage is given by Eq. (22). The measured output voltage vs. duty cycle characteristics are plotted in Fig. 15, and agree well with theory.

A transient output voltage waveform was also measured. The converter was operated at constant duty cycle, and a step load change from 15Ω to 30Ω was applied. The measured output voltage transient is shown in Fig. 16a, and the waveform

predicted by Eq. (34) is plotted in Fig. 16b. The 120Hz voltage ripple is also visible in these waveforms. Agreement is again good.

Open-loop ac line voltage and current waveforms are plotted in Fig. 17. These were measured with a line voltage of 120V rms, a duty cycle of 0.21, and an output power of 40W. The EMI filter components consisted of a 16.7 mH inductor and a 0.47 μF capacitor. The line current waveform is indeed nearly sinusoidal and in phase with the line voltage.

Thus, operation of the DCM flyback converter as a loss-free resistor, in a high power factor rectification application, has been verified experimentally. Input port, output port, and control characteristics have been proven, and a transient response has been correlated with theory.

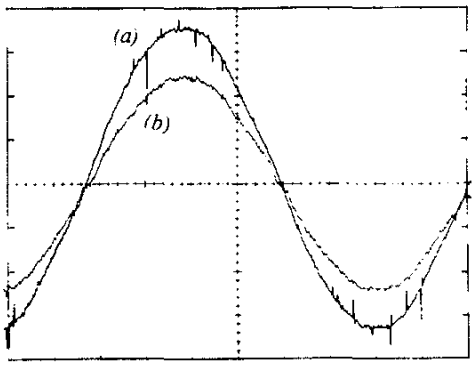

Fig. 17. Measured input line voltage and current waveforms: (a) line voltage, 50V/div, (b) line current, 0.2A/div. Horizontal scale: 2ms/div.

8. Conclusions

The input port of a discontinuous conduction mode flyback or buck-boost converter inherently emulates a resistor, and hence no additional control is needed to obtain high power factor rectification. Isolation, transformer turns ratio, and low parts count can also be obtained.

The basic functions which any high power factor rectifier must perform, namely ac input port resistor emulation, efficient transfer of input power to the output port, and control of power flow, are described in a simple and intuitive way by the "loss-free resistor" two-port network. Further, the discontinuous mode buck-boost and flyback converters naturally behave as loss-free resistors. This concept is used here to solve for the system waveforms, obtain design equations, and derive small signal ac models of flyback rectifier systems.

The ac small signal models derived here neglect both high frequency switching ripple and 120 Hz rectification ripple, and are suitable for design of the slow output voltage feedback loop. Both resistive loads and closed-loop dc-dc voltage regulator loads can be modelled. Careful design of the control loop is necessary to prevent excessive transient peak output voltages.

It is well understood that the voltage feedback loop must operate slowly; how slowly is quantified here. A simple first-order estimate of the line current harmonic distortion shows that the percent third harmonic content is approximately equal to the ratio of 120 Hz duty cycle variation amplitude to the quiescent duty cycle. A similar result holds for the phase shift of the fundamental. Hence, degradation of the line current waveform quality can be alleviated by reduction of the 120 Hz feedback gain.

Experimental results confirm the validity of the loss-free resistor model, and the operation of the open-loop flyback converter as a high power factor rectifier.

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