Abstract- An analytical averaged equivalent circuit model is derived revealing how dominant loss mechanisms vary with converter operating point in a PWM converter. The model is based on the operational characteristics of power diodes and IGBTs. Laboratory experiments support the derived model and confirm that IGBT current tailing and diode reverse-recovery are indeed the most critical losses in a PWM converter. These losses are more significant at light load, hence reducing the energy capture of converters used in wind generation.

I. INTRODUCTION

Power electronic converters in wind generators operate under the requirement of high efficiency at light load. This requirement is not necessary in most conventional applications, provided that the total power loss is no worse than at maximum load. This unique requirement in wind generation applications evolves from the very nature of operation of typical wind turbines. Because wind turbines may operate for long periods of time under low wind speed conditions, variable-speed wind generators may show significant degradation in energy capture capability when using PWM converters of low efficiency at light load. Hence, the phenomenon and origins of lower efficiency at light load need to be studied in depth to achieve better energy conversion rates.

If losses vary linearly with output power, then the converter efficiency is independent of load. Conduction losses of typical PWM inverters vary linearly with or as the square of output power, and hence cannot explain the observed efficiency degradation at light load. As described in this paper, switching losses typically exhibit a less-than-linear dependence on output power. Hence, reducing the output power does not proportionately reduce the switching loss. In particular, the switching loss induced by diode reverse-recovery has been found to dominate at light load.

The averaged switch modeling approach [1,2] is employed here, to explain how the major loss mechanisms vary with converter operating point. Averaged switch models of two-level and three-level PWM converters have been derived and analyzed. These models incorporate simple approximate relationships that describe how switching loss parameters vary with the converter operating point. These relationships are based on physical understanding of semiconductor devices, and have been verified in the laboratory.

In Section II, the important switching loss mechanisms are described, and the first-order dependencies of the switching loss parameters are derived. The results of extensive laboratory tests to measure these dependencies are summarized in Section III. Averaged switch models of two-level and three-level converters are developed in Section IV. The predictions of these models for a variable-speed wind generation application are discussed in Section V.

II. SWITCHING LOSS MECHANISMS

Switching loss can be resolved into components induced by the diode reverse-recovery mechanism, the IGBT current-tailing phenomenon, the IGBT turn-on time, and the output capacitances of the IGBTs and diodes. Each mechanism leads to energy loss that is a function of the semiconductor on-state current and off-state voltage:

\[ W_p = \text{Energy loss induced in IGBT by diode reverse-recovery} \]
\[ W_{	ext{tail}} = \text{Energy loss during IGBT turn-off transition, owing to current tail} \]
\[ W_r = \text{Energy loss during IGBT turn-on transition, during rise of collector current} \]
\[ W_c = \text{Energy loss induced in IGBT by semiconductor output capacitances} \]

The sum of these switching energy losses, multiplied by the switching frequency, is equal to the average switching power loss. Thus, the total switching loss is directly proportional to switching frequency.

A. DIODE REVERSE-RECOVERY

Well-known waveforms for the turn-off transition of a silicon diode are illustrated in Fig. 1. While the diode conducts, it contains stored minority charge of magnitude \( Q \) dependent on the forward current \( I_F \). This minority charge must be removed before the diode can become reverse-biased. There are two mechanisms for removal of this charge: passive removal through recombination inside the diode, and active removal through negative diode current. The amount of charge that recombines is dependent on the rate \( \text{dldt} \) at which the diode current changes during the turn-off transition, which in turn depends on the IGBT turn-on switching speed and stray inductances. The remaining stored charge is actively removed. The actively removed charge is called the “recovered charge” \( Q_r \). During the reverse-
recovery time, of length \(t_r\), negative current flows through the diode, the diode remains forward-biased, and the instantaneous power loss in the transistor is very high. The voltage \(V_f\), in Fig. 1, is the dc link voltage (i.e., \(V_g = V_t\)).

The functional dependence of \(Q\) and \(t_r\) on the diode forward current \(i_f\) is determined by the physical mechanisms within the diode, [3,4]. At very low current, Shockley-Read-Hall recombination dominates the diode behavior, and the dependence of the stored charge \(Q\) on the forward current can be approximated as linear. For intermediate currents (i.e., the usual operating range of the diode), injection efficiency typically dominates the device behavior, and \(Q\) varies as the square root of forward current. For very large currents, Auger recombination may become dominant, leading to a cube root dependence of \(Q\) on forward current. The recovered charge \(Q_r\) and reverse-recovery time \(t_r\) will be proportional to \(Q\).

The result is that the forward current can be represented as a third-order polynomial function of \(Q\). Since injection efficiency usually dominates over the normal operating range of the power diode, a simpler approximation is to simply let \(Q\) be proportional to the square root of the forward current:

\[
Q = k_{Qf} \sqrt{I_F} \tag{2}
\]

This less-than-linear dependence means that stored charge is only a weak function of on-state current. Hence, the switching loss arising from the diode reverse-recovery mechanism will have a greater impact on efficiency as the load power is reduced. The coefficient \(k_{Qf}\) is also a function of the junction temperature and the turn-off \(di/dt\).

The relationship between the on-state stored charge \(Q\) and the recovered charge \(Q_r\) depends on rate of change \(di/dt\) of the diode current during the IGBT turn-on transition. If \(di/dt\) is very high (tending towards a step change of diode current), then \(Q_r = Q\). It may then be possible to expect the recovered charge \(Q_r\), to depend on \(I_F\) in the same way as \(Q\):

\[
Q_r = k_{Qr} \sqrt{I_F} \tag{3}
\]

Lower rates of \(di/dt\) cause a significant amount of the stored charge to recombine during the diode turn-off process, so that \(Q_r < Q\). The quantities \(Q_r\) and \(t_r\) then additionally depend on \(di/dt\). For very slow \(di/dt\), \(Q_r\) and \(t_r\) become independent of \(I_F\) and are functions solely of \(di/dt\).

The reverse-recovery time \(t_r\) is related to the recovered charge \(Q_r\), according to

\[
t_r = \sqrt{\frac{Q_r (1+S)}{(di/dt)}} \tag{4}
\]

where \(S\) is the “snappiness factor” of the diode and is determined by the physical diode construction [5]. The above equation is derived in numerous texts and is sometimes quoted on manufacturer’s data sheets. Derivation of this equation is based solely on the geometry of the waveforms of Fig. 2, and is not dependent on the internal construction of the diode. Equations (3) and (4) predict that, for fixed \(di/dt\), the diode reverse-recovery time \(t_r\) should vary with on-state current \(I_F\) according to

\[
t_r = k_{t_r} \sqrt{I_F} \tag{5}
\]

where \(k_{t_r}\) is a proportionality coefficient that is a function of \(di/dt\).

This is a very weak dependence. Thus \(t_r\) can be accurately modeled as independent of on-state current \(I_F\). Equation (4) further suggests that \(t_r\) varies as the inverse square-root of \(di/dt\); this is also a weak dependence, but variations in \(t_r\) may be measurable if \(di/dt\) varies significantly.

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**Fig. 2** Theoretical variation of diode stored charge with on-state current, and the dominant physical mechanisms.

**B. IGBT CURRENT TAILING**

The IGBT can be viewed as a MOSFET cascaded by a PNP bipolar junction transistor. When the IGBT conducts, part of its current flows through the effective MOSFET, while the remainder flows through the PNP; the ratio of these two currents is determined by the device construction.
During the turn-off transition, the MOSFET turns off very quickly, and its share of the on-state current is therefore interrupted quickly. However, the current of the PNP continues to flow until the stored minority charge within the n' region has recombined.

The IR data sheets for recent devices [6] illustrate that $Q_{\text{tail}}$ exhibits a linear dependence on the on-state current, $I_F$. Current tailing can be the largest single loss mechanism of an IGBT inverter and any dependence of $Q_{\text{tail}}$ is critical. It is assumed here that simple recombination leads to a linear dependence:

$$Q_{\text{tail}} = k_{Q} I_F$$

This linear dependence implies that the effect of current tailing on inverter percent efficiency is independent of load power.

C. IGBT TURN-ON LOSS

Significant losses can also be observed during the rise time of the collector current during the IGBT turn-on transition. During this interval, the gate driver charges the gate capacitance of the IGBT. At high currents, some time may be required to supply minority charge to the effective PNP transistor within the IGBT, further slowing the turn-on transition. Time $t_{\text{on}}$ is required for the IGBT collector current to rise from zero to the inductor current $I_L$; during this time, the diode remains on and the IGBT collector-to-emitter voltage remains fixed at the dc link voltage $V_{dc}$.

Assuming a constant slope rise, $dI/dt$, of the collector current, then it is possible to form the following equations:

$$\frac{I_{F}}{t_{\text{on}}} = \frac{dI}{dt}$$

$$W_F = \frac{V_{g} I_{F} I_{\text{on}}}{2} = \frac{V_{g} I_{F}^2}{2(dI/dt)}$$

As was mentioned previously, it was observed that $dI/dt$ decreases at large load currents and low dc link voltage. This causes the energy loss induced by this mechanism to increase significantly at high current. The loss during the turn-on transition is not significant at light load current and high voltage, because of the strong dependence on $I_F$ and because $dI/dt$ is dominated by the fast switching of the effective IGBT MOSFET at low current.

D. DEVICE OUTPUT CAPACITANCES

The output capacitances of the IGBT and diode are nonlinear elements, whose incremental values vary approximately as the inverse square root of applied voltage. The energy stored in these capacitances is lost in the IGBT during the IGBT turn-on transition.

As illustrated in Fig. 5, each inverter phase contains two IGBTs and two diodes, each of which exhibits output capacitance. During the turn-on transition of the upper IGBT, the lower diode turns off and undergoes the reverse-recovery process. The switching loss caused by the output capacitance of the lower diode is included in the reverse-recovery computations discussed in subsection (A) of this section. However, it remains to include the energy stored in the capacitances of the upper diode and both IGBTs.

The incremental output capacitance of an IGBT or diode can be modeled by a function of the form

$$C = \frac{dq}{dv} = \frac{C_o}{V_{\text{max}}}$$

This model is sufficiently accurate for computation of the switching losses induced by output capacitance. The constant $C_o$ is extracted from the incremental capacitance specified on the manufacturer’s data sheet. $V$ is the applied collector-to-emitter or cathode-to-anode voltage. The energy stored in the output capacitance is found by integration of (8), as follows:

$$W_c = \int v dv = \int_0^{V_{\text{max}}} C_o \cdot \frac{V_{\text{max}}}{V_{\text{max}}} = 2C_0 \frac{V_{\text{max}}^{1.5}}{5}$$

where $V_{\text{max}}$ is the off-state voltage of the device. In a dc-link inverter, this loss is a function of the dc link voltage but is independent of current. Hence, this loss is independent of power throughput.

MOSFETs tend to exhibit higher output capacitances than IGBTs or diodes, because of the relatively large chip area of similarly rated MOSFETs. In consequence, this source of switching loss is more significant in MOSFET inverters than in systems containing IGBTs. Nonetheless, it can be a significant loss at light load operating conditions.

III. LABORATORY EXPERIMENT

In the laboratory, efficiency and loss tests were performed on the power stage illustrated in Fig. 3. The circuit was operated at various constant values of duty cycle $D$, dc link voltage $V_{dc}$, and dc current $I$. Losses in each semiconductor device were separately measured. This data was then used to predict losses when ac modulations are present. 1200V devices were employed. The IGBTs were International Rectifier IRGPHS0F with ratings of 42A at 25°C, 25A at 100°C. The power diodes were International Rectifier HFA30PB120 ultrafast with ratings of 30A average.

![Fig. 3 One phase of a two-level PWM inverter circuit](image-url)
IGBT switching times and diode stored charge exhibit a significant temperature dependence. To obtain an accurate model, it is necessary to operate the semiconductor devices at a fixed junction temperature [3,4]. Each semiconductor device was mounted on a separate heatsink. Several power resistors are mounted on the same heatsink, and were driven by an adjustable voltage source with known power. This thermal system was calibrated by applying a known dc power to the IGBT. Given the manufacturer’s published junction-to-case thermal resistance, the case temperature required to produce a given junction temperature can be calculated. The external resistor power was increased until this case temperature is attained. The relationship between resistor power, case temperature, and the semiconductor device power dissipation is then known. The thermal systems for each IGBT and diode were calibrated in this manner.

Switching losses were measured in two ways: (a) the thermal approach described above, and (b) using oscilloscope waveforms. Good agreement between the two methods was obtained. Based on the measured data, the model parameters listed in Table 1 were obtained. It was found that IGBT turn-on switching time and IGBT output capacitance did not lead to significant switching loss, while the other modeled losses were significant.

### TABLE 1

<table>
<thead>
<tr>
<th>MODEL PARAMETERS, BASED ON EXPERIMENTAL DATA</th>
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<tbody>
<tr>
<td>$V_{sat} = 1.34$ V</td>
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<tr>
<td>$V_D = 1.50$ V</td>
</tr>
<tr>
<td>$Q_r = (2.3 \times 10^{-8}) \times \frac{\langle i_2(t) \rangle_{T_s}}{\langle v_1(t) \rangle_{T_s}}$</td>
</tr>
<tr>
<td>$t_r = (8.0 \times 10^{-8}) \times \frac{\langle i_2(t) \rangle_{T_s}}{\langle v_1(t) \rangle_{T_s}}$</td>
</tr>
<tr>
<td>$Q_{tail} = 3.0 \times 10^{-7} \times \langle i_2(t) \rangle_{T_s}$</td>
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### IV. AVERAGED SWITCH MODELING

#### A. TWO-LEVEL CONVERTER MODEL

Figure 4 illustrates one phase of a conventional two-level PWM inverter circuit switch network, and Fig. 5 shows its typical switching waveforms. The salient features shown on the waveforms are defined as follows:

- $t_r$: Diode reverse-recovery time
- $t_{on}$: Current rise time, IGBT turn-on transition
- $t_s$: IGBT on-state conduction time
- $V_{sat}$: IGBT forward voltage drop
- $V_D$: Diode forward voltage drop
- $Q_{tot}$: The sum of the diode recovered charge $Q_r$ and the total charge $Q_s$ stored in the output capacitances of the IGBTs and reverse-biased diodes
- $Q_{tail}$: Integral of the collector current waveform during the current fall time (area of the current tail)

For positive current, $I_F$, the upper IGBT and lower diode conduct. The average values of the upper IGBT voltage and current waveforms of Fig. 5, for positive $I_F$, are equal to

$$
\langle v_{ce} \rangle_{T_s} = \frac{T_s - t_1}{T_s} (V_g + V_D) + \frac{t_1}{T_s} V_{sat}
$$

$$
\langle i_c \rangle_{T_s} = \frac{t_1 + t_r + \frac{1}{2} t_{on}}{T_s} I_F + \frac{Q_{tot} + Q_{tail}}{T_s}
$$

The idealized waveforms of Fig. 5 ignore voltage rise and fall times, and assume hard-recovery diodes. The notation $\langle x \rangle_{T_s}$ denotes the average value of $x$, averaged over the switching period $T_s$.  

![Fig. 4 Two-level converter switch network](image)

![Fig. 5 IGBT voltage and current waveforms (I_F>0)](image)
where the effective transistor duty cycle is $D = \frac{t_{s}}{T_{s}}$ and $D' = 1 - D$.

An averaged equivalent circuit model corresponding to (13) and (14) is illustrated in Fig. 6(a). A similar procedure leads to the model of Fig. 6(b), for negative current. These models represent the low-frequency components of the terminal waveforms of the switch network. The average input and output powers are correctly represented. The effective 1:D transformer models the conversion of power from the input to the output ports of the switch network. Switching losses are modeled with the two current sources. $Q_{r}$ is the diode recovered charge, $Q_{\text{null}}$ is the area of the IGBT current tail, and $t_{s}$ is the diode reverse-recovery time. Diode and IGBT voltage drops are modeled as two voltage sources and two resistors in the secondary side of the circuit model. Note that each source consumes power, hence reducing the switch network efficiency. The charge $Q_{r}$ was found to be smaller than $Q_0$ in our laboratory experiment; hence $Q_{\text{null}} = Q_{r}$. Notice also that the term $t_{\text{null}}$ has been discarded from the averaged model due to its negligible effect.

![Diagram](image.png)

**Fig. 6** Averaged circuit models of the PWM switch network of Fig. 4

**B. THREE-LEVEL CONVERTER MODEL**

The averaged switch approach can also be applied to model the dependence of efficiency on load in other PWM converters. A three-level inverter circuit, also known as a neutral-point clamped PWM inverter [7], illustrated in Fig. 7, is modeled using a procedure similar to that used in the previous subsection.

Figure 8 illustrates the resulting averaged switch model of the upper half of the three-level converter circuit. As in Fig. 6, the effective 1:D transformers model the conversion of power from the input to the output ports of the switch network. Figure 8 (a) models the network for positive $i_{2}$, when $Q_{1}$ and $D_{3}$ switch with pulse-width modulation. Figure 8 (b) models the network for negative $i_{2}$, when $Q_{1}$ and $D_{1}$ are pulse-width modulated. Models for the lower half of the three-level switch network are symmetrical.

![Diagram](image.png)

**Fig. 7** One phase of a three-level inverter circuit

![Diagram](image.png)

**Fig. 8** Averaged circuit models for the upper half of the three-level PWM switch network of Fig. 7

**V. DISCUSSION**

The model of Fig. 6 and the parameter values of Table 1 were used to predict the efficiency of a two-level PWM dc-link rectifier/inverter system, Fig. 9, in a variable-speed wind generation application. Generator power is assumed to vary as the cube of turbine speed. The dc link voltage is a fixed 825 V, and the 60 Hz ac system voltage is 480 V three phase. The generator voltage varies between zero and 480 V. The model was solved analytically for sinusoidal pulse-width modulation, and the average input and output powers of the switch network were computed. Unity power factor was assumed. Predicted efficiencies of the PWM rectifier and inverter stages are plotted in Fig. 10, for a switching frequency of 10 kHz. Notice how efficiency drops rapidly at light load; a typical obstacle in variable speed wind generators. The rectifier efficiency is lower than the inverter efficiency because the rectifier must operate with a lower ac-side voltage and hence with higher currents. The composite efficiency is the products of the rectifier and inverter efficiencies. This plot includes the losses of the semiconductor devices only; losses of the reactive elements and control circuitry are not included.
Losses in one phase of the rectifier are detailed in Fig. 11. It can be seen that, at 10 kHz and lower output powers, the losses caused by the diode reverse-recovery and IGBT current tail are most significant, followed by conduction losses. Hence switching losses dominate at light load, especially the diode reverse-recovery loss. The reduced efficiency at light load can therefore be ascribed to the less-than-linear dependence of diode reverse-recovery loss on load current.

Figure 12 illustrates the more severe switching losses that are observed when the switching frequency is doubled. Therefore, converter efficiency is also lower at 20 kHz as illustrated in Fig. 13.

Figures 11 and 12 describe how dominant loss mechanisms vary with converter operating point. Variation of switching loss mechanisms with operating point is central to the issue of wind inverter efficiency at low wind speed.

Figure 14 shows variations in efficiency of a three-level rectifier/inverter system operating at 10 kHz. Figure 15 shows the corresponding distribution of losses in the converter at 10 kHz. As in Fig. 10-13, the previously developed averaged switch model of the three-level converter as well as the laboratory acquired model parameters have been used to generate these plots. With a three-level converter, we are able to double the DC link voltage and thus double the maximum possible load power. The increase in conduction loss is associated with the increase in the number of switching devices in the three-level converter. The switching loss is reduced because of the decreased
semiconductor voltage stresses. Figure 16 and 17 illustrate the same three level converter characteristics at 20 kHz.

![3-Level Converter Efficiency vs. Load Power at 10 kHz](image)

**Fig. 14** Three-level converter efficiency vs. load power at 10 kHz

![3-Level Converter Loss Summary at 10 kHz](image)

**Fig. 15** Sources of loss in three-level converter (per phase) at 10 kHz

![3-Level Converter Efficiency vs. Load Power at 20 kHz](image)

**Fig. 16** Three-level converter efficiency vs. load power at 20 kHz

![3-Level Converter Loss Summary at 20 kHz](image)

**Fig. 17** Sources of loss in three-level converter (per phase) at 20 kHz

Wind generators operate most often at a fraction of their rated power. For example, a typical wind distribution may be centered at 25% to 35% of rated power. It is critical to the economic success of wind generation that output kWh be maximized, and hence system efficiency at power levels well below rated power is extremely important [8]. The requirement of high efficiency at light load is unique to wind generation. In other applications, efficiency of the electrical machines and power converters at light load is not important, provided that the total power loss is no worse than at maximum load. Indeed, the efficiency of a typical PWM converter is maximum at a point near rated load power, and falls off rapidly at light load. This behavior can significantly degrade the energy captured by a variable-speed wind generator. Hence, there is a need to develop a better understanding of the mechanisms that degrade efficiency at light load, and to create new approaches to optimizing converter efficiency over a wide range of load powers.

In this paper, we presented experimentally verified averaged switch models for two-level and three-level PWM converters. By incorporating the extensively tested model parameters of Table 1 into the developed averaged switch models, we were able to relate variations in converter efficiency to variations in converter operating point. These changes in efficiency were further explained in terms of changes in converter’s most significant loss mechanisms. At light load, losses due to the diode reverse-recovery mechanism were observed to dominate. Comparing the plots presented in Section V of this paper provides the necessary insight needed prior to selecting the specific components and converter type for a given PWM converter design.

**VI. CONCLUSION**

**REFERENCES**